DRIVEMODE

Integrated Modular Distributed Drivetrain for Electric & Hybrid Vehicles

Document title: Simulation Report

D4.2: Report 1 with simulation results
WP 4, T 4.4

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This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement N°769989

DRIVEMODE

Technical references

Project Acronym	DRIVEMODE
Project Title	Integrated Modular Distributed Drivetrain for Electric & Hybrid Vehicles
Project Coordinator	Mikko Pihlatie VTT Technical Research Centre of Finland mikko.pihlatie@vtt.fi
Project Duration	November 2017 – October 2020 (36 months)

Deliverable No.	D4.2
Dissemination level*	PU
Work Package	WP 4 - Converter
Task	T4.4 – Modeling and Simulation
Lead beneficiary	8 (TUI)
Contributing beneficiary/ies	2 (Semikron), 3 (Visedo)
Due date of deliverable	31 October 2018
Actual submission date	DD October 2018

* PU = Public

PP = Restricted to other programme participants (including the Commission Services)

RE = Restricted to a group specified by the consortium (including the Commission Services)

CO = Confidential, only for members of the consortium (including the Commission Services)

v	Date	Comment	Author	Beneficiary
0.1	09/10/2018	Initial draft	Nathalie Becker	TUI
0.2	18/10/2018	Internal review	Roland Bittner	Semikron
0.3	18/10/2018	TMT review	Katrin Wand	AVL
0.4	22/10/2018	Commented	Alexander Smirnov	VTT
0.5	22/10/2018	Corrected Version	Nathalie Becker	TUI
0.6	23/10/2018	TMT review	Katrin Wand	AVL
0.7	23/10/2018	Final draft	Nathalie Becker	TUI
1.0		Final check and submission	Mikko Pihlatie	VTT

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Executive Summary

This report summarizes the thermal simulations, fluid simulations and corresponding optimizations done for the converter. The report explains the optimizations process of the converter from the starting point up to the nearly finalized and optimized version. The aim of the different optimization steps was to improve the thermal performance of the converter. Optimization especially in regard of temperature gradients and decreasing of the chip temperature were done. Because too high temperatures lead to a number of problems and can have a substantial impact on performance and reliability. The last section of the document gives an outlook on future optimization steps and planned additional studies.

The simulations were done in the DRIVEMODE work package 4 (WP 4), Converter, task 4.4, Modeling and simulation.

Attainment of the objectives and if applicable, explanation of deviations

This report is a summary of performed simulations and optimizations in regard of thermal performance and fluidic flow for the converter in WP4. It contains the individual steps of the thermal and fluidic optimization process and gives an outlook to future simulations and possible optimizations. Therefore all relevant objectives for this deliverable were achieved.

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Nomenclature

SiC	Silicon Carbide
Version 1	The first design idea
Version 2	The test structure to investigate the chip distance
Version 3	The test structure with 3 power hybrids
Version 4	A nearly finalized design
Power Hybrid	Assembled AMB substrates
AMB	Active Metal Bonding

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1. Introduction

1.1 Introduction Drivemode

DRIVEMODE is a project funded by the European Commission under the Horizon 2020 framework. The project aims at designing a compact modular integrated drive module (IDM) for pure electric vehicles (PEVs) and hybrid electric vehicles (HEVs).
The IDM developed in the DRIVEMODE project will be a drivetrain platform that then can be adopted depending on the application e.g. demonstration vehicle. The modularity and scalability of the IDM will be used to support a wider range of application. This document will
Report on the thermal and fluid simulations performed for the converter including corresponding optimizations with regard to thermal performance.

1.2 Scope of document

This report is a summary of the finished thermal and fluid simulations for the converter as well as a summary of several design iterations to optimize the thermal behavior.

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2. Thermal and fluid simulations

2.1 Simulation conditions

The simulations presented in this report were performed under the following conditions:

- Power dissipation per chip: 80 W
- Cooling fluid temperature at the inlet: 65°C
- Flow rate : 10 L/min
- Consideration of thermal paste and sinter paste
- Ambient pressure : 1.01325 bar
- Interface wall between fluid and solid : smooth wall
- Turbulence of the fluid: Laminar flow

These conditions were defined and agreed together with the project partners. The power dissipation of 80 W per chip is based on 35 A_{rms} per chip. This value was maintained during the simulations and subsequent optimization steps to ensure a better comparability of the result. The final version will be simulated with the final current requirements. Currently the feasibility of the design for higher current requirements is checked on an extrapolation basis.
The CAD models of the converter and the heat sink were constructed in SolidWorks. The thermal and fluid simulations were performed in the ANSYS Workbench environment. A schematic drawing of the simulation model is pictured in figure 1.

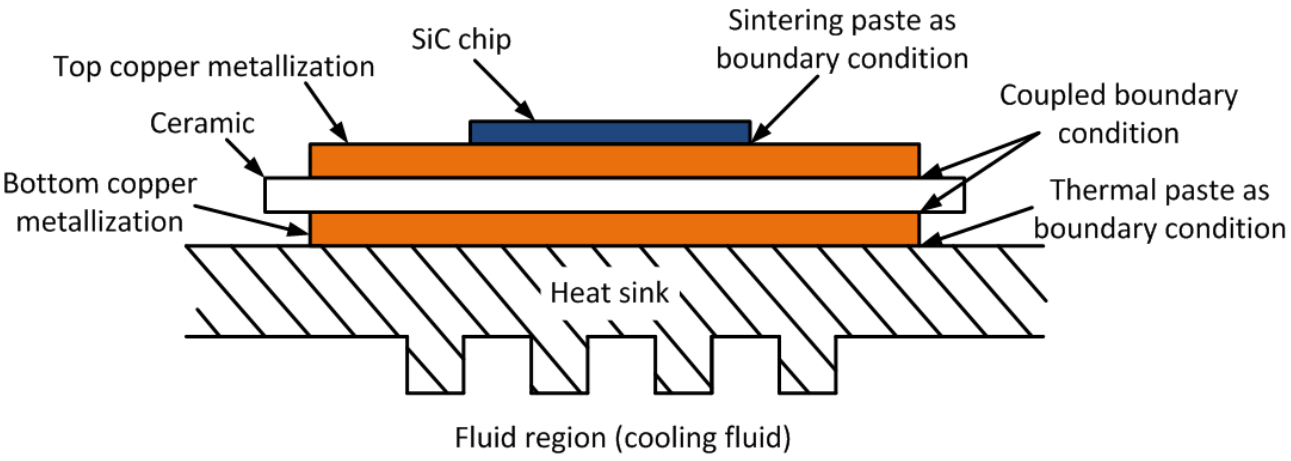

Figure 1: Schematic drawing of the simulation model

The inverter is simulated by means of a FEM simulation. The simulations performed were steady state thermal simulations coupled with fluid dynamic simulations. This was done to properly simulate the heat conduction coefficient at the interface of the fluid and solid region.
Coupled heat conduction takes place at the interfaces of the solid bodies. Additionally at the interface between SiC chip and upper copper metallization sinter paste is assumed as 2D material (fig. 1). Located at the interface between lower copper metallization and heat sink is heat conducting paste as 2D material (fig. 1). The flow of the coolant through the heat sink is calculated using the Shear stress transport model.

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2.2 First thermal considerations

2.2.1 Background

For the very first thermal studies a design idea of the partner Semikron has been used. This design will be referred to as version 1. This design is optimized in regard of a high packaging density with SiC chips and possibilities for improvement should be explored. Version 1 was simulated in combination with a pin fin heat sink to evaluate the thermal performance. In figure 2 the CAD model of the module on top of the original Heat sink is shown.

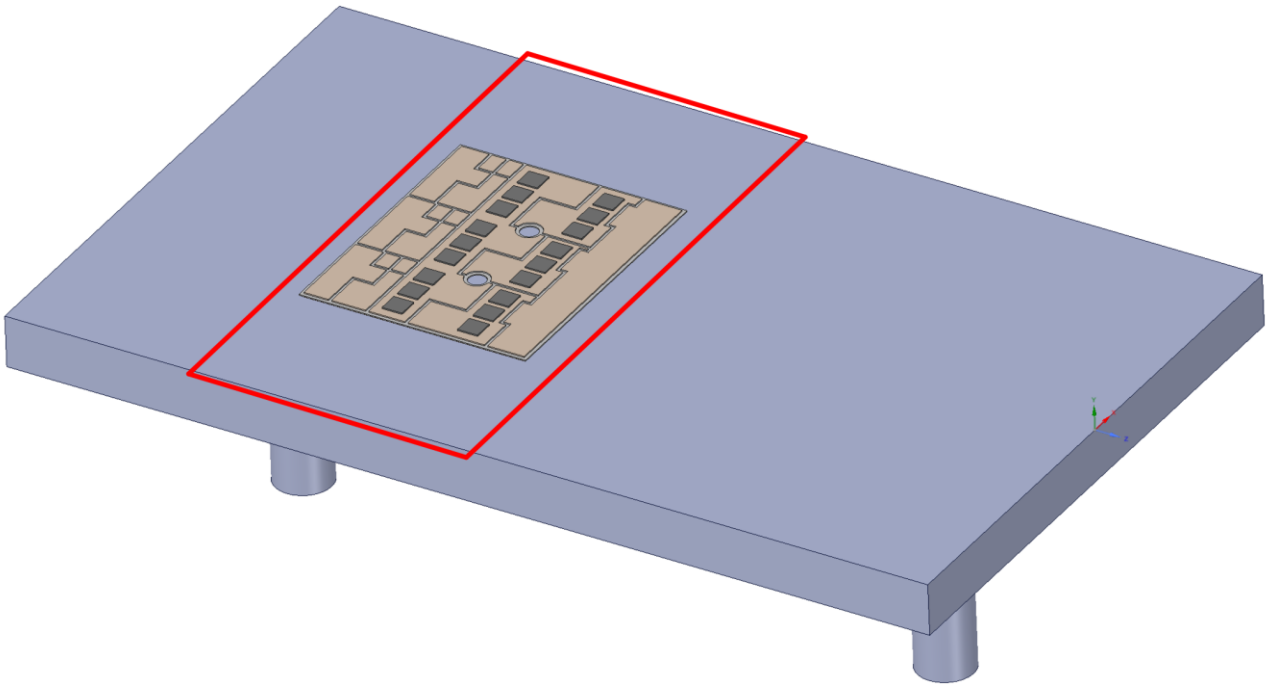

Figure 2: CAD model of version 1

The Inlet and outlet are located centrally on the underside of the opposite narrow sides. The position of the module on top of the heat sink was adjusted. Now the cooling fluid meets the module from the top side and passes the TOP and BOT chips of each phase evenly. Figures 3 and 4 show the simulation results of the module in combination with the new heat sink. Figure 3 shows the thermal contour of the section marked in Figure 2.

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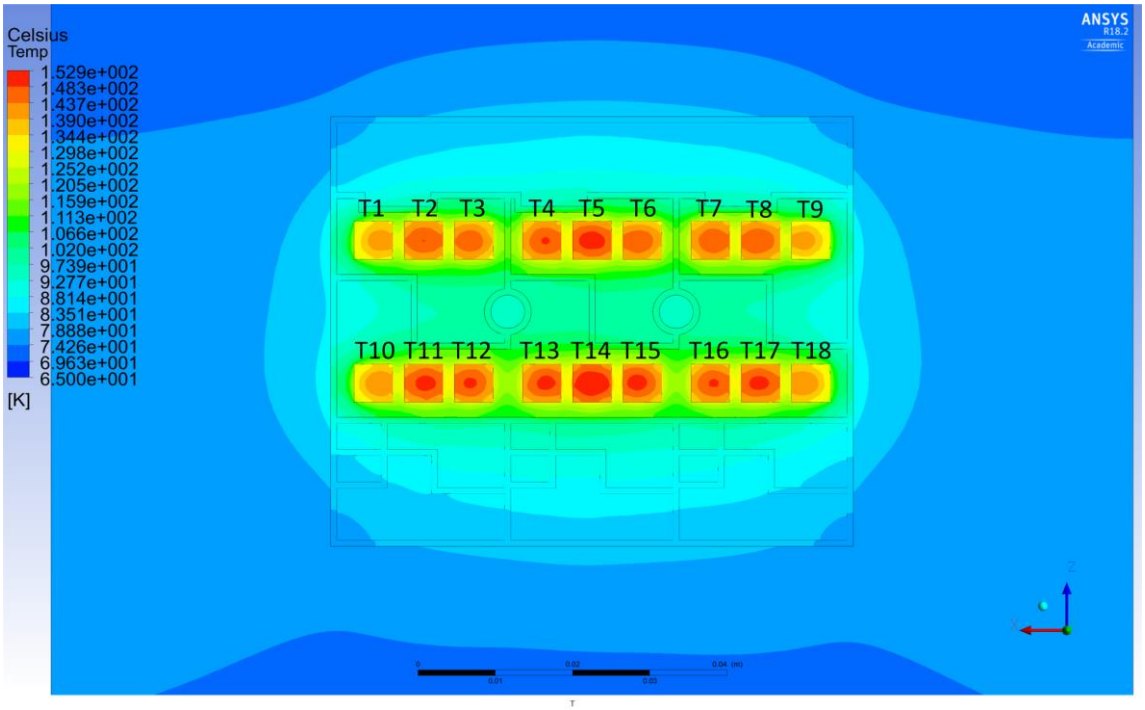

Figure 3: Thermal contour of the power hybrid

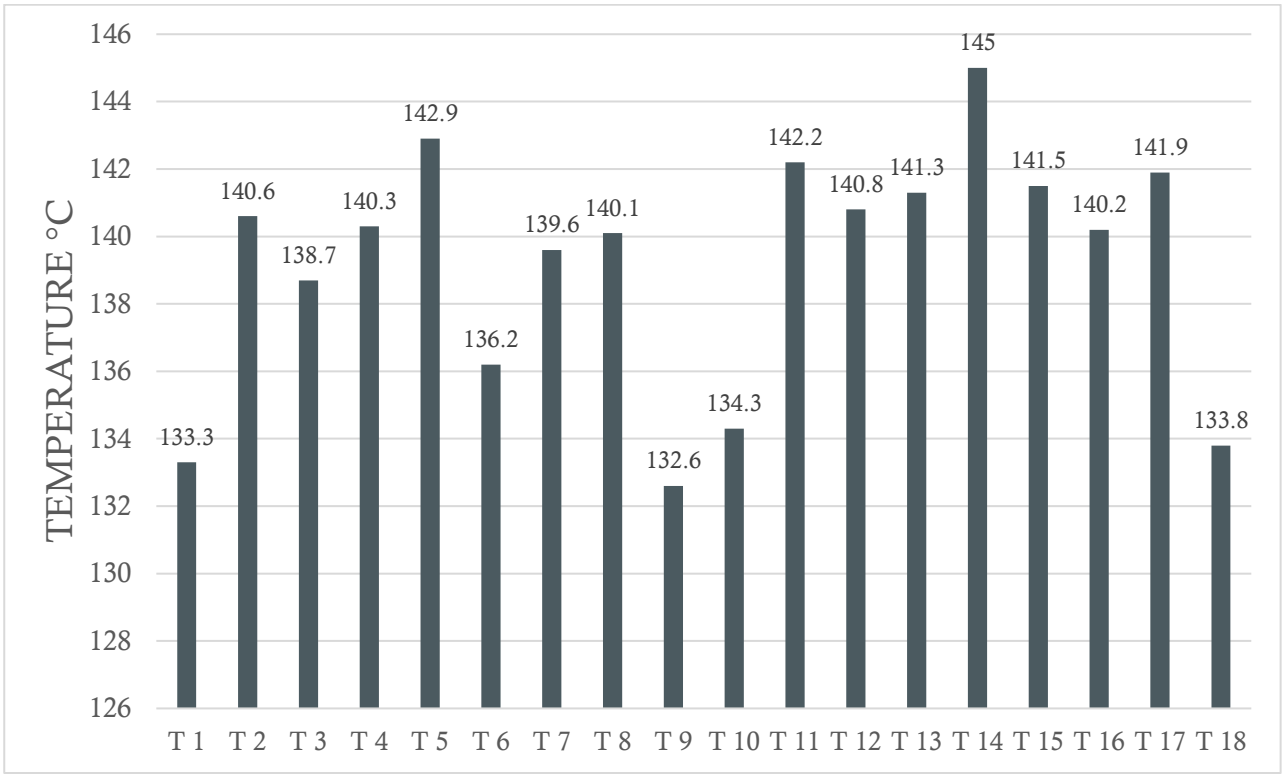

Figure 4: Bar chart of the average chip temperatures

As one can see from the simulation results (fig. 3 and fig. 4) the heat distribution of the chips is very unevenly. It was expected that the chips in the middle get hotter than the ones located at the outer phases. But the temperature difference of 12.4 °C between the hottest and coolest chip is very large. A large temperature difference leads to an asymmetrical current distribution and that's not desired. Besides if one chip gets hotter than the others, the performance of the whole

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system is limited by this chip. Furthermore the temperature of the hotspot is with 152.9 °C is too high. Since the motor requirements of the motor have been increased, the chips have to be cooler to still meet the requirements with 3 chips. The visible temperature difference between TOP and BOT results from the heating of the cooling water under the module.
Various possibilities for thermal improvement were investigated:

1. Increasing the pressure drop around the pin area
2. Different fin geometries in the heat sink (e.g. oval, square)
3. Increasing the chip distance to decrease the mutual thermal influence

The increase of the pressure drop is only useful up to a certain limit. In a small study the pressure drop was varied my means of the pin geometry and the corresponding R_{th} was calculated. The graph in figure 5 shows the relationship between pressure drop and R_{th} of the heat sink.

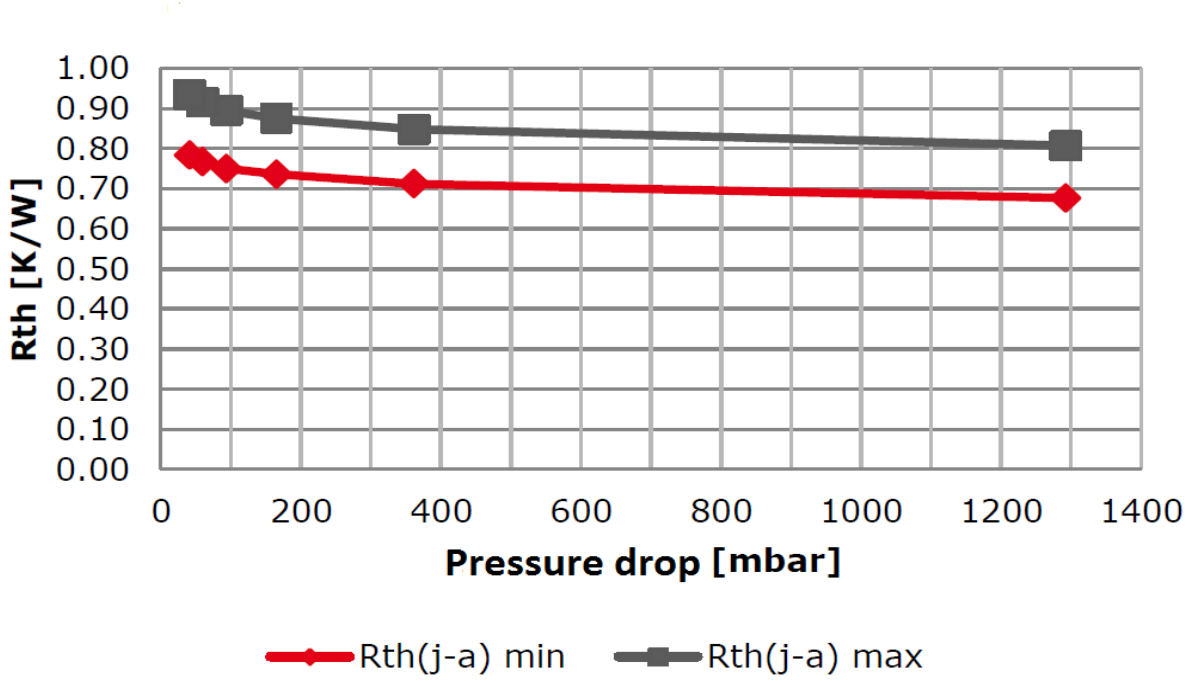

Figure 5: Dependence of R_{th} and pressure drop

The relationship between R_{th} and pressure drop is proportional to $\frac{1}{x}$. Therefore, increasing the pressure drop is only useful up to a certain limit. For the proposed heat sink this limit is between 200 to 400 mbar.

Instead of using pin fins in the heat sink the use of oval or square pins are possible and can lead to an improvement of the cooling performance. But due to the better manufacturability pin fin had been selected.

The last point about increasing the chip distance was the most promising one to improve the thermal performance of the module. This idea was the subject of further investigations, which will be presented in the chapters 3 and 4.

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2.3 First iteration: Variation of the chip distance

To investigate the influence of the chip distance a simple test structure (version 2) was designed (Fig. 5).

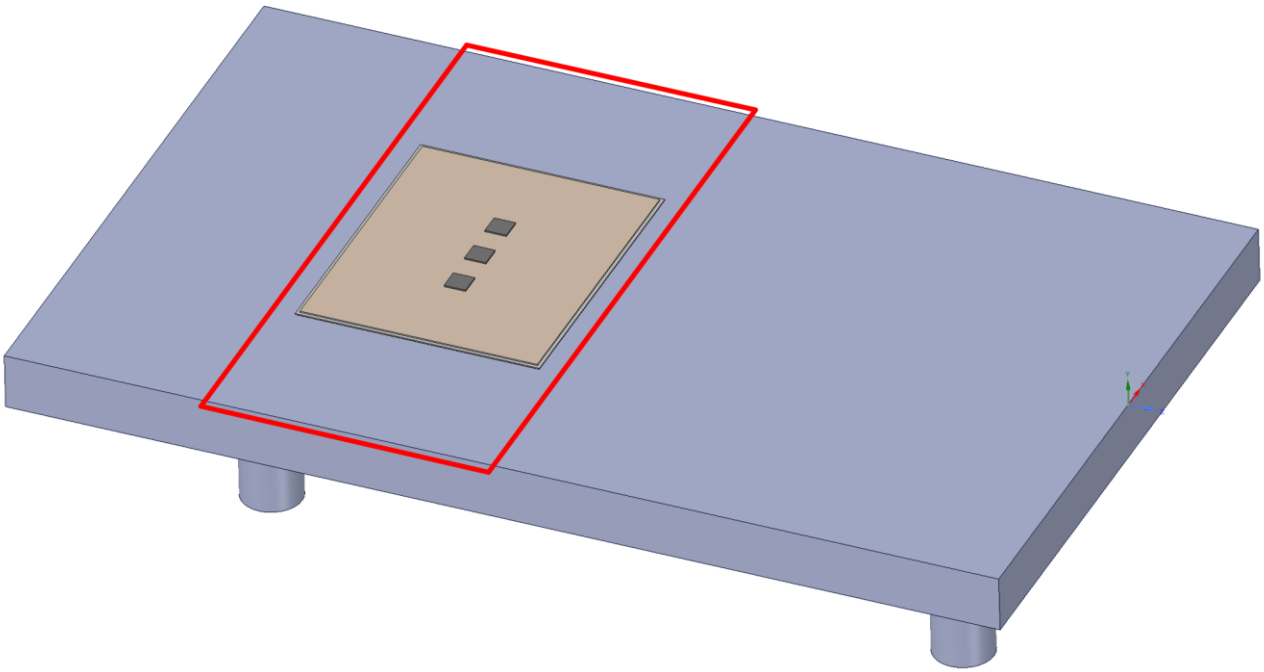

Figure 6: CAD model of version 2

This test structure consists of the same heat sink as the one in version 1 (fig. 2) and a simplified version of the module. The simplified module is a ceramic substrate materialized with full-surface copper layers on the upper and lower side and three SiC chips. The test structure was simulated under the in chapter 1 specified conditions. A total of 8 simulations were carried out with different chip distances starting from 1 mm up to 8 mm in 1 mm steps. Originally the simulations were performed up to 10 mm but no significant change could be observed between 8 mm and 10 mm. Thus it was decided to use 8 mm as the upper limit of the simulation. The simulation results can be seen in the figures 7 to 10. Figures 7 and 8 picture the thermal contours marked in figure 6.

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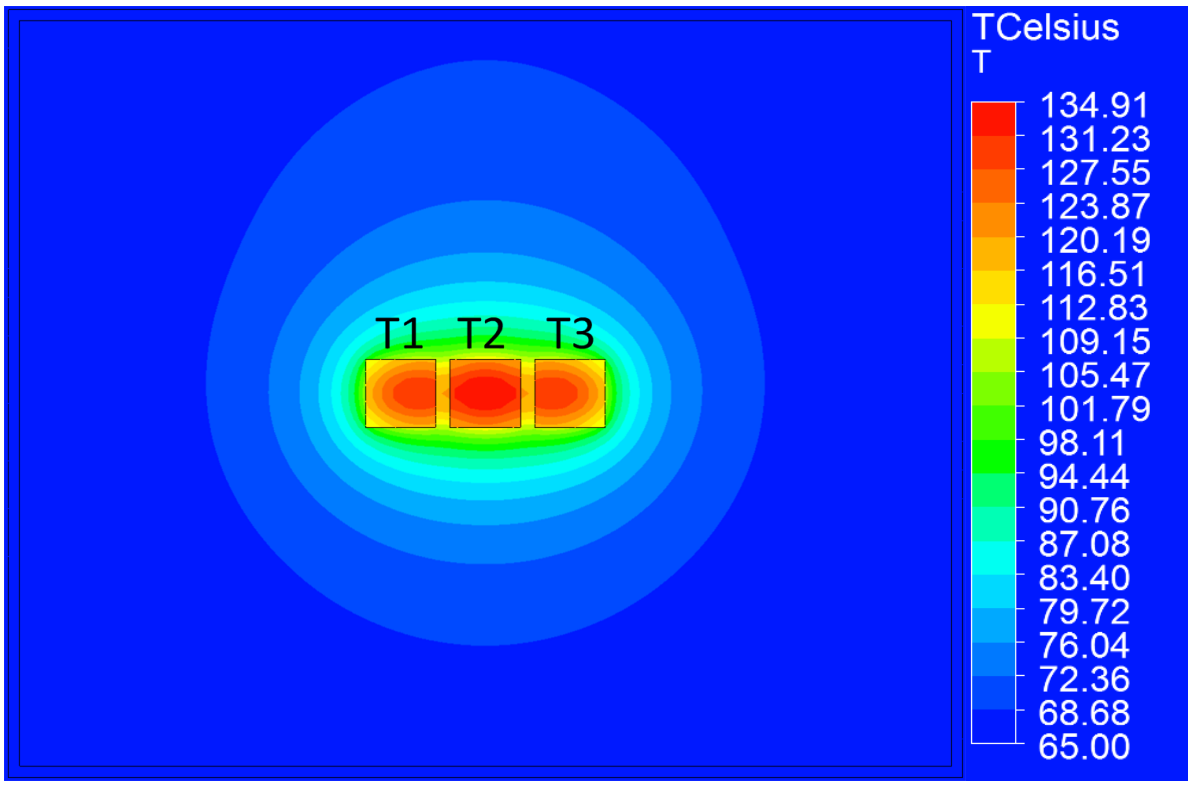

Figure 7: Thermal contour of the test structure for 1 mm chip distance

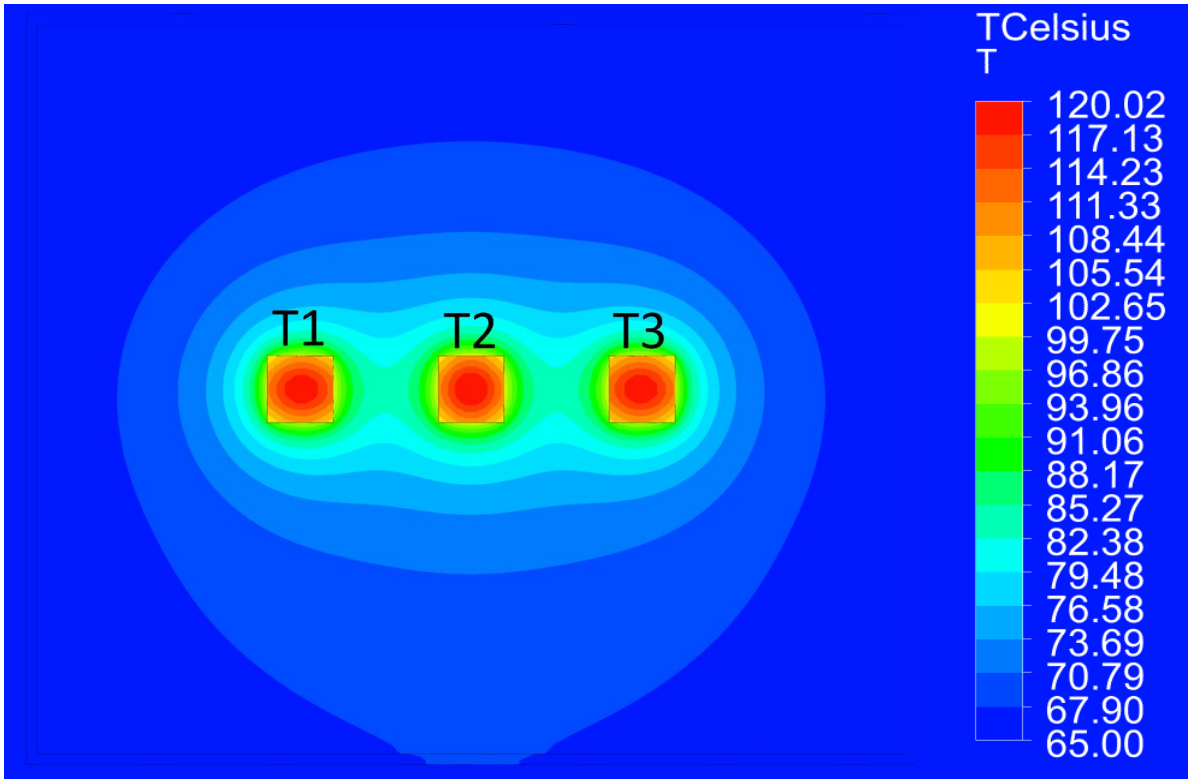

Figure 8: Thermal contour of the test structure for 8 mm chip distance

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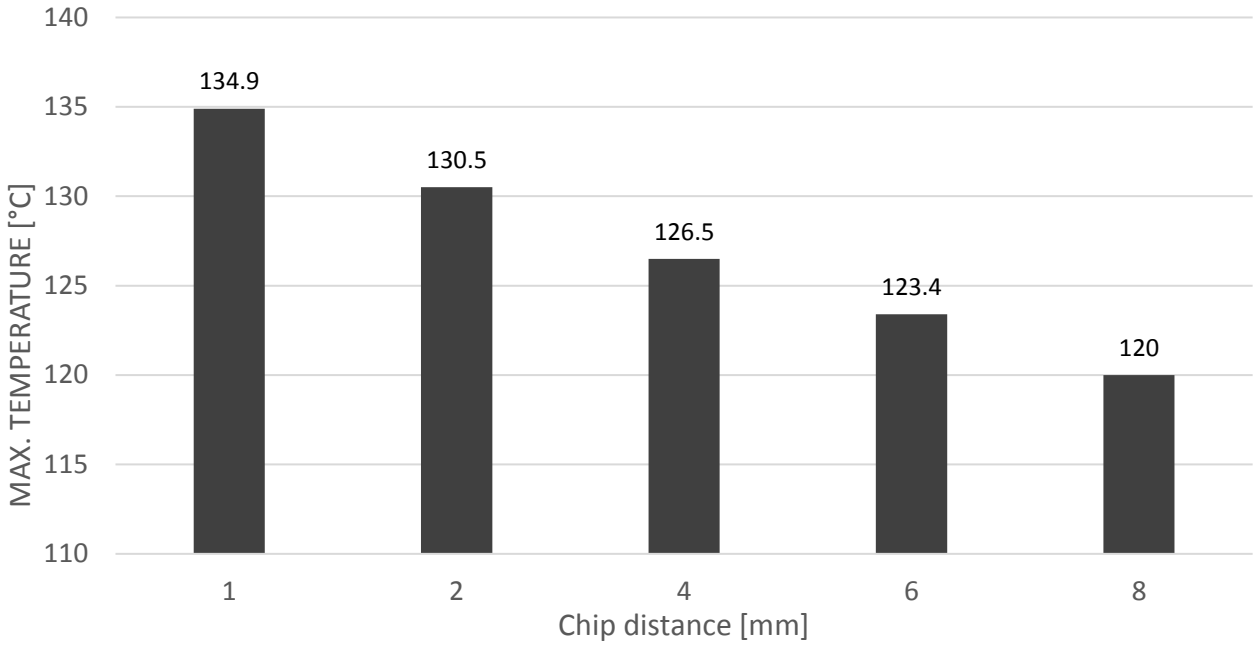

Figure 9: Development of the hotspot temperature

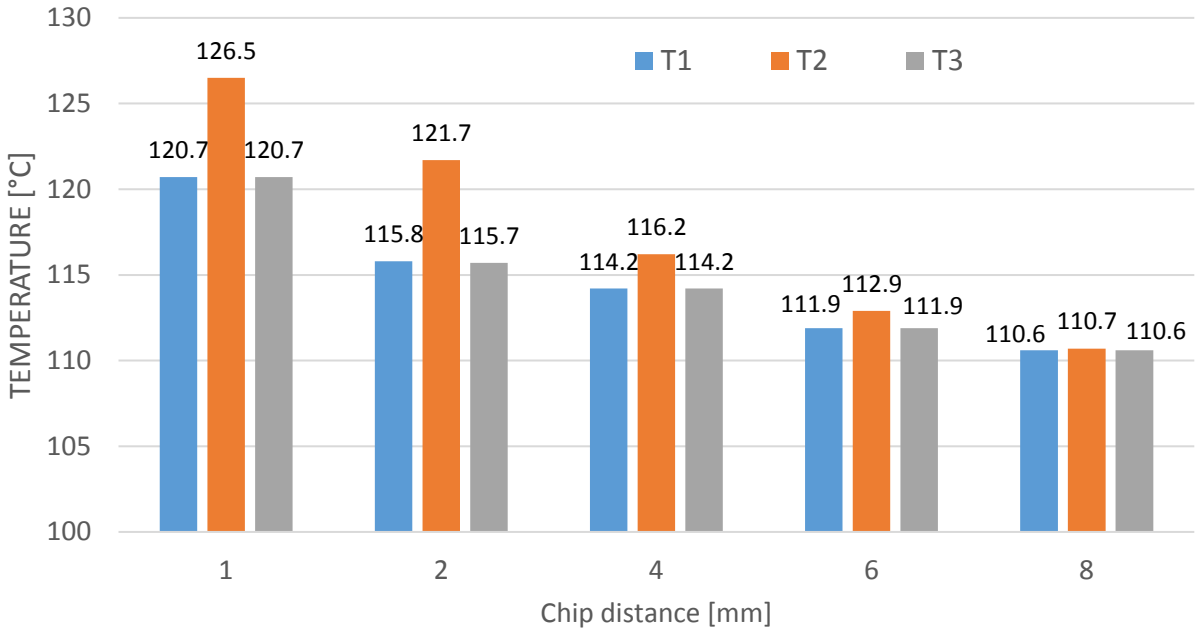

Figure 10: Development of the average chip temperature

Figure 7 shows the thermal contour plot of the test structure with a chip distance of 1 mm. It is apparent that the thermal coupling between the chips is intense. Furthermore the temperature difference between the chips is with 5.8 °C (Fig. 9) nearly as large as in the original module (Fig. 3).
In figure 8 one can see the same test structure with a chip distance of 8 mm. At a distance of 8mm hardly any mutual influence between the chips could be observed. Furthermore the temperature of the hotspot decreases from 134.9 °C to 120 °C.

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The Bar charts in figures 9 and 10 illustrate the development of the hotspot and the average chip temperature in relation to the chip distance. As expected the hotpot temperature in figure 9 decreases gradually with increasing chip distance by 14.9 °C. The average chip temperature in figure 10 shows a similar behavior. An interesting observation is that the temperature difference between the chips gradually disappears as the distance increases. At a distance of 8 mm the temperature difference is nearly gone. This leads to an even current distribution among the chips and the performance of the system is not limited by one chip anymore.
Despite the larger chip spacing, the active area of version 2 is still smaller than that of a comparable IGBT module. In addition, the overall size of the inverter is primarily determined by the area required for control and driver.
Because of the numerous advantaged it was decided to use an enlarged chip distance in further investigations.

2.4 Second iteration: Construction on 3 separate power hybrids

Next to an enlarged chip distance it was also decided to construct the 3 phases on 3 separate power hybrids (version 3). Half bridge configurations with a single phase per power hybrid are very common due to the possibility of flexible use in H-Bridge configuration e.g. for DC-DC-converters, and Six-Pack or Multi-phase configurations for use in motor inverter. In addition the division into 3 separate ceramics offers some advantages. The first advantage is the thermal decoupling between the 3 phases. Secondly, the 3 phases can be tested separately from each other and offer an easier handling. And last the pretested half bridges enable higher production yield due to minimized effect of single failures. The heat sink used was the version with pin fins introduced in chapter 2. Figure 11 pictures the modified module with 3 separate power hybrids.

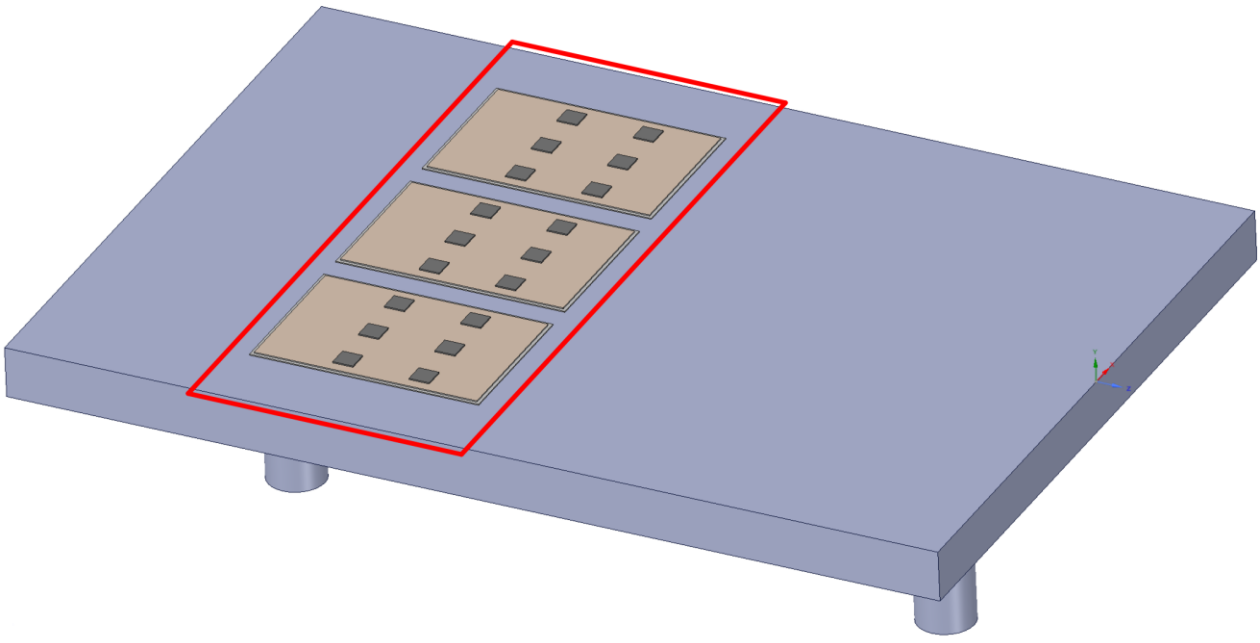

Figure 11: CAD model of version 3

The thermal behavior was simulated under the conditions presented in chapter 1. Additionally the new version was simulated with different chip distances, starting with 1.5 mm (distance of

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the original version) to 8 mm. This was done to verify that 8 mm was still the best choice. One can see the simulation results in figures 12 to 15.

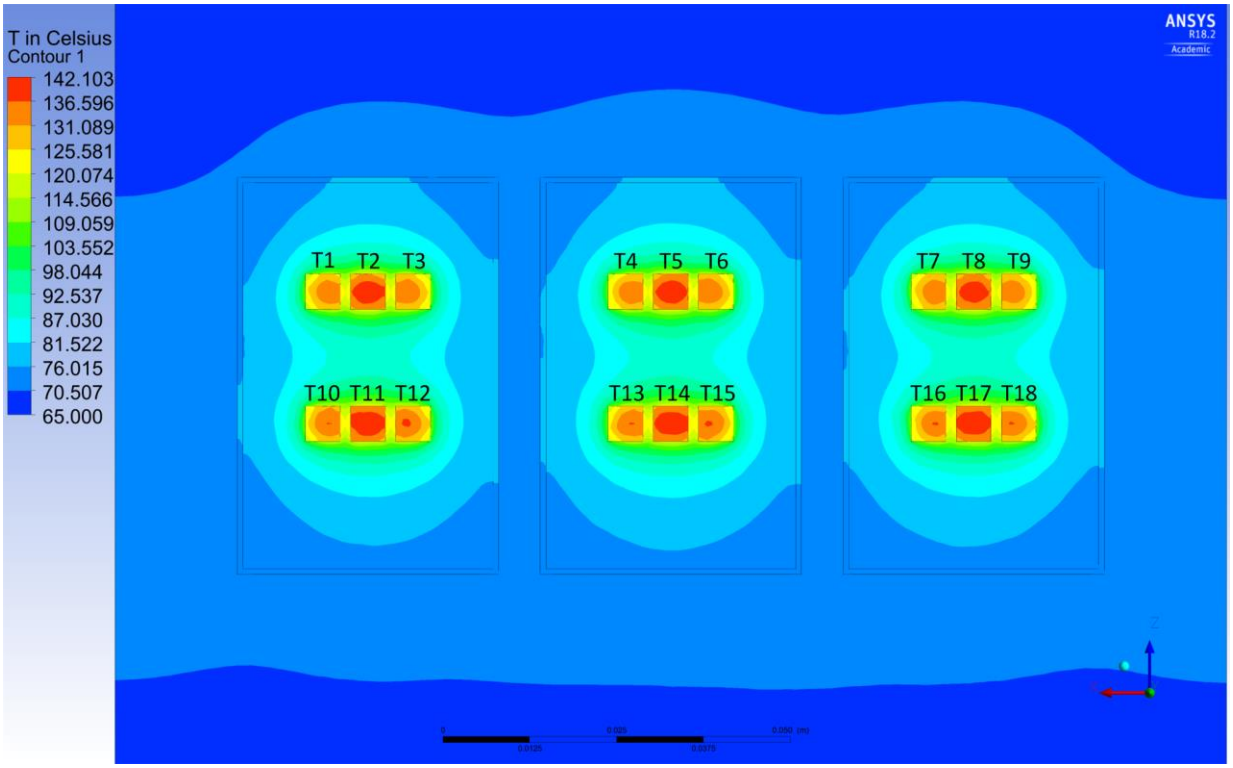

Figure 12: Thermal contour of the power hybrids with a chip distance of 1.5 mm

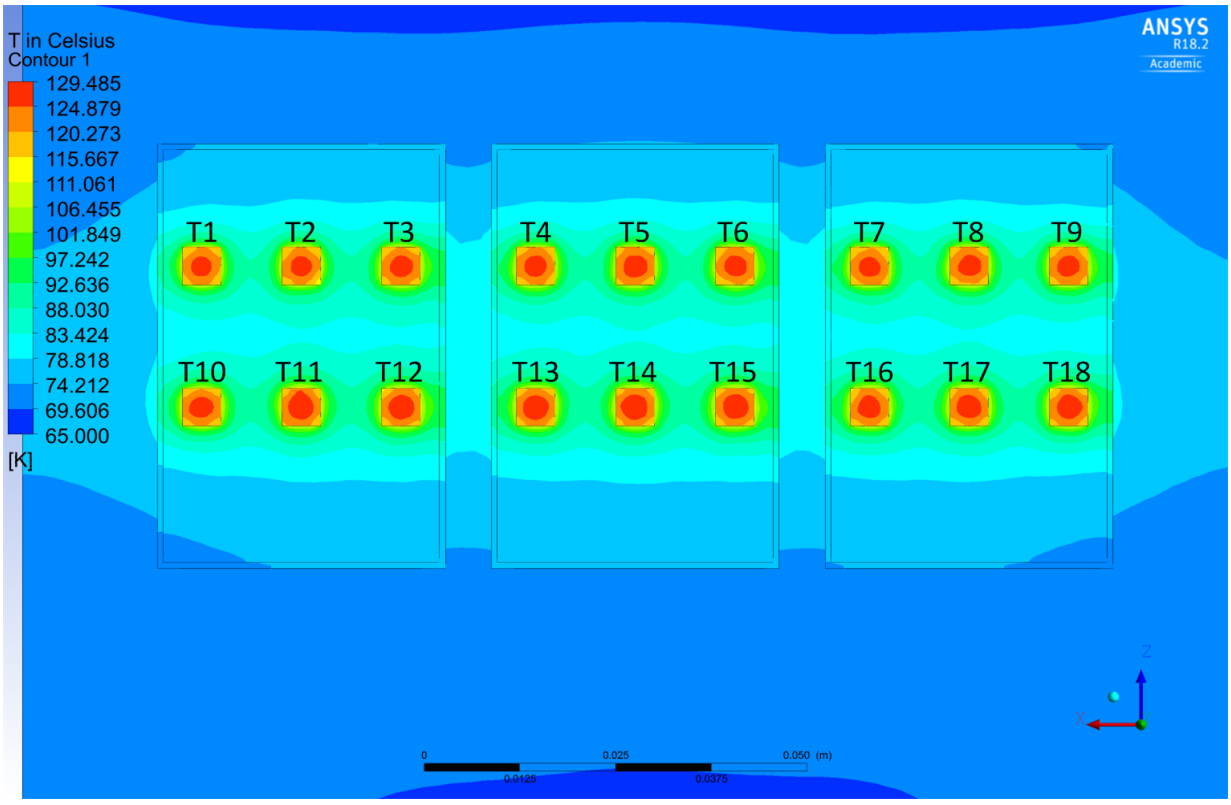

Figure 13: Thermal contour of the power hybrids with a chip distance of 8 mm

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Figures 12 and 13 show the thermal contours of the modified module with a chip distance of 1.5 mm and 8 mm. As with the previous simulations in chapter 3, a chip distance of 8 mm is the best choice for this version of the module as well. In the figures 14 and 15 one can see that the hotspot temperature and the average chip temperature decrease with increasing chip distance.

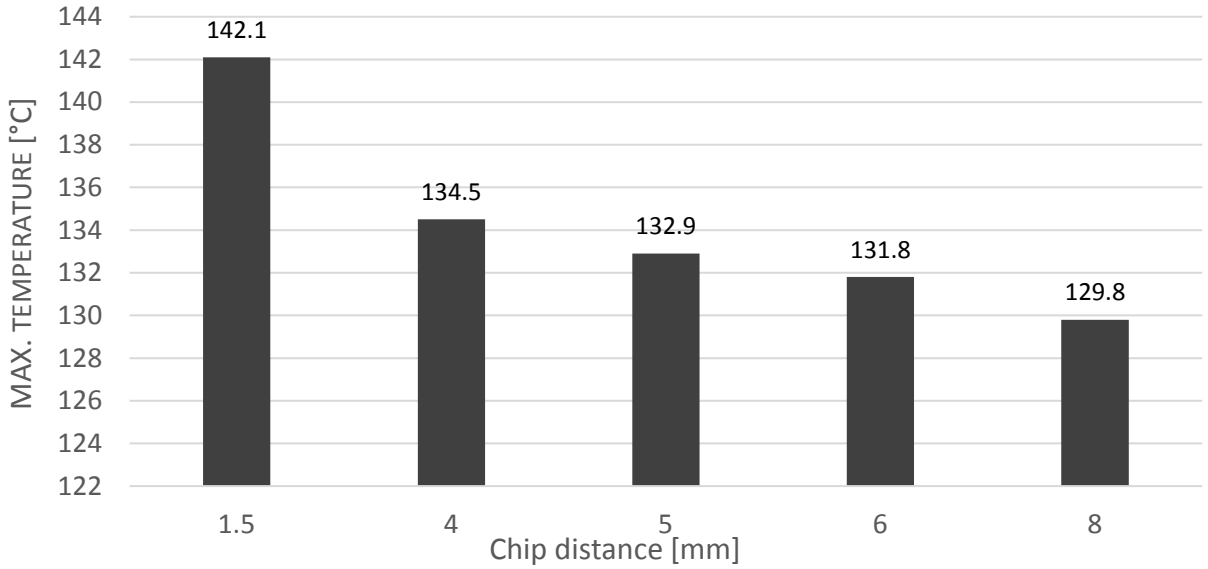

Figure 14: Development of the hotspot

The hotspot in this version is with 129.8 °C a little bit hotter than the hotspot in the test structure from chapter 3. The reason is that the chips in the middle are heated by the outer chips. The same behavior as in chapter 3 can be observed with the average chip temperature in figure 15. The average temperature decreases until at 8 mm the chips are thermally decoupled and have approximately the same temperature.

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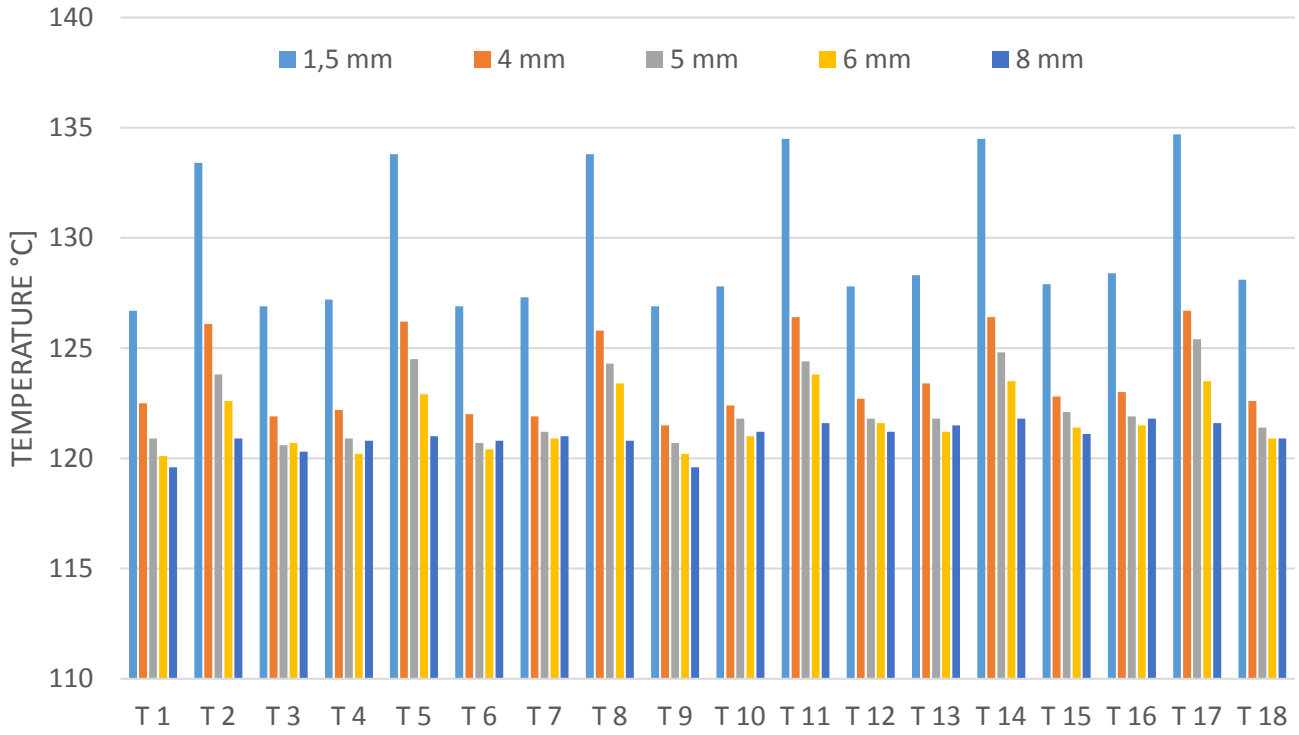

Figure 15: Development of the average chip temperature

The bar charts in the figures 16 and 17 show a comparison between the version 1 from chapter 2 and the recent modified version 3.

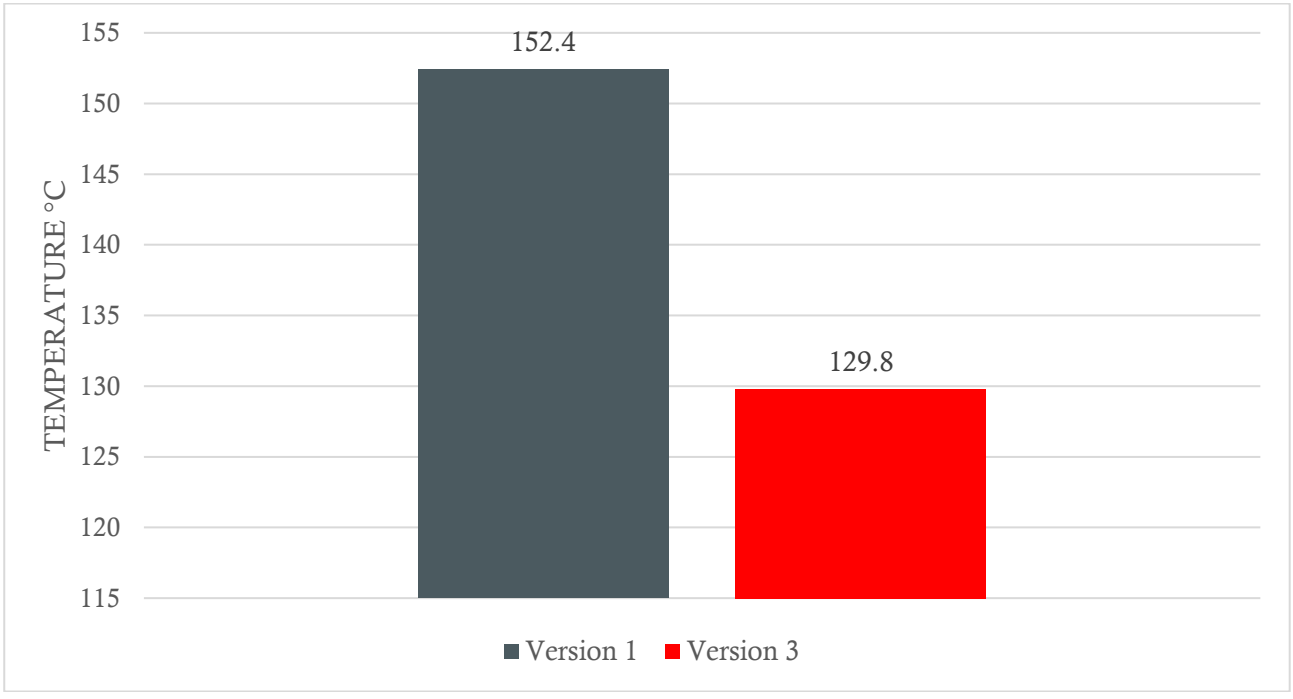

Figure 16: Comparison of the hotspot temperature of version 1 and version 3

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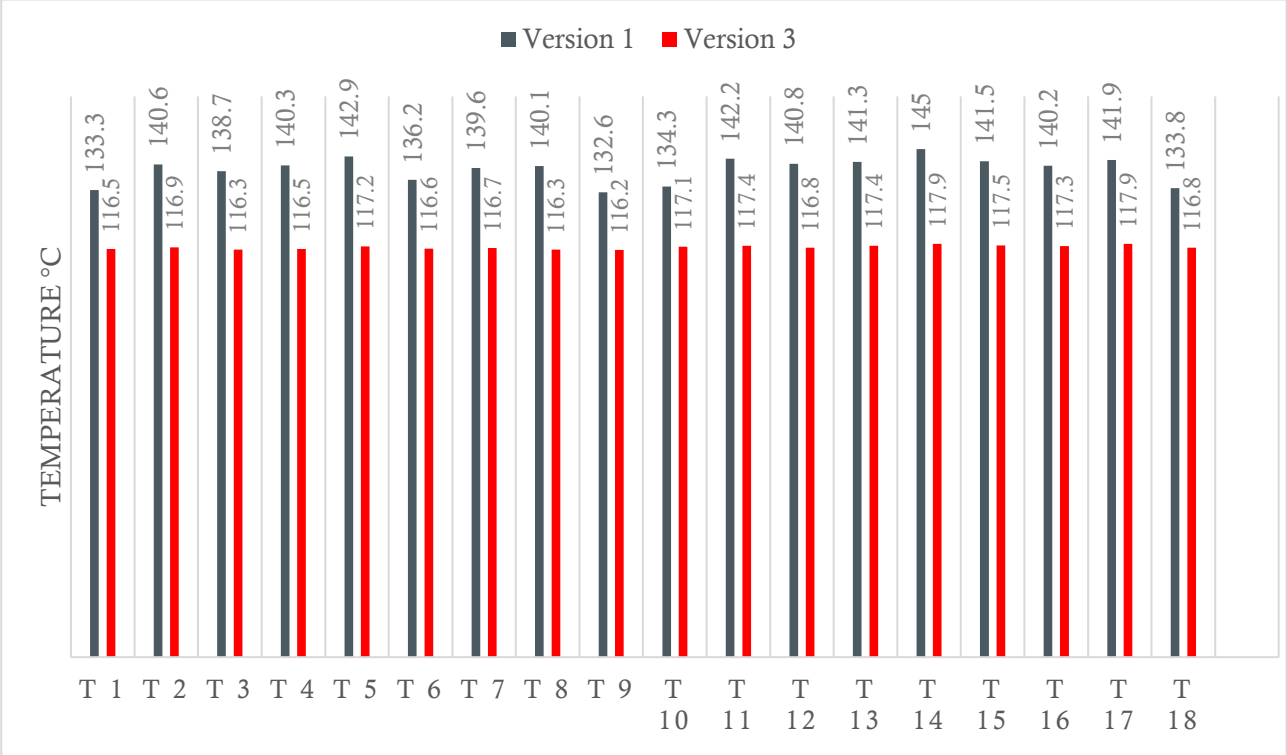

Figure 17: Comparison of the average chip temperature of version 1 and version 3

The temperature of the hotspot could be reduced by 23.1 °C, which corresponds to an improvement of 16%. A similar picture can be seen when comparing the average chip temperature. Here an improvement of 18.2 °C could be achieved, which corresponds to an improvement of 14%. The reduction of hotspot temperature and average chip temperature means that we can carry more power with the same chip area.
In summary, the simulation show that increasing the chip distance brings a lot of advantages and significant improvement compared to the original module.

2.5 Third iteration: Variation of thermal paste and heat sink material

2.5.1 Thermal paste

In the previous simulations, a heat conduction paste with a relatively poor heat conduction coefficient (WLP1) was used. To further improve the thermal performance of version 3 a different thermal paste with a better heat conduction coefficient was investigated (WLP2). The thermal paste is located between the power hybrids and the heat sink. Figures 18 and 19 show a comparison of the simulation results of the different materials.

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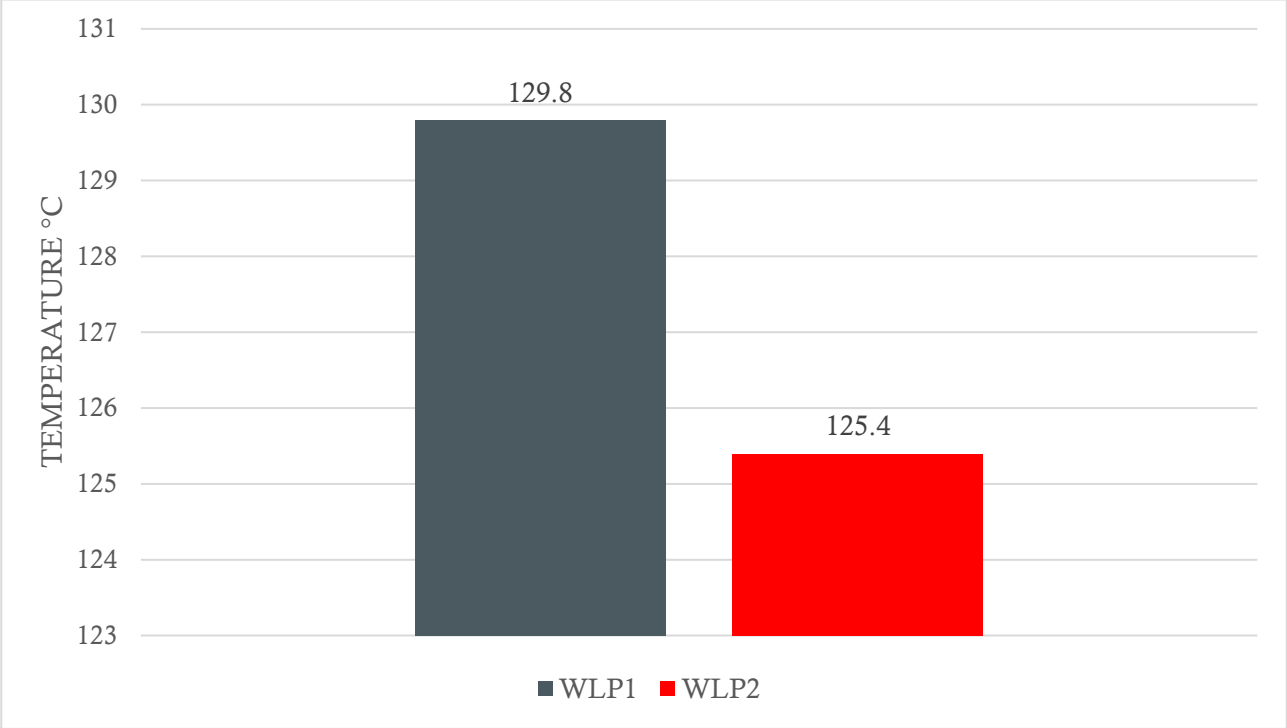

Figure 18: Comparison of the hotspot temperature between a power hybrid with WLP1 and WLP2

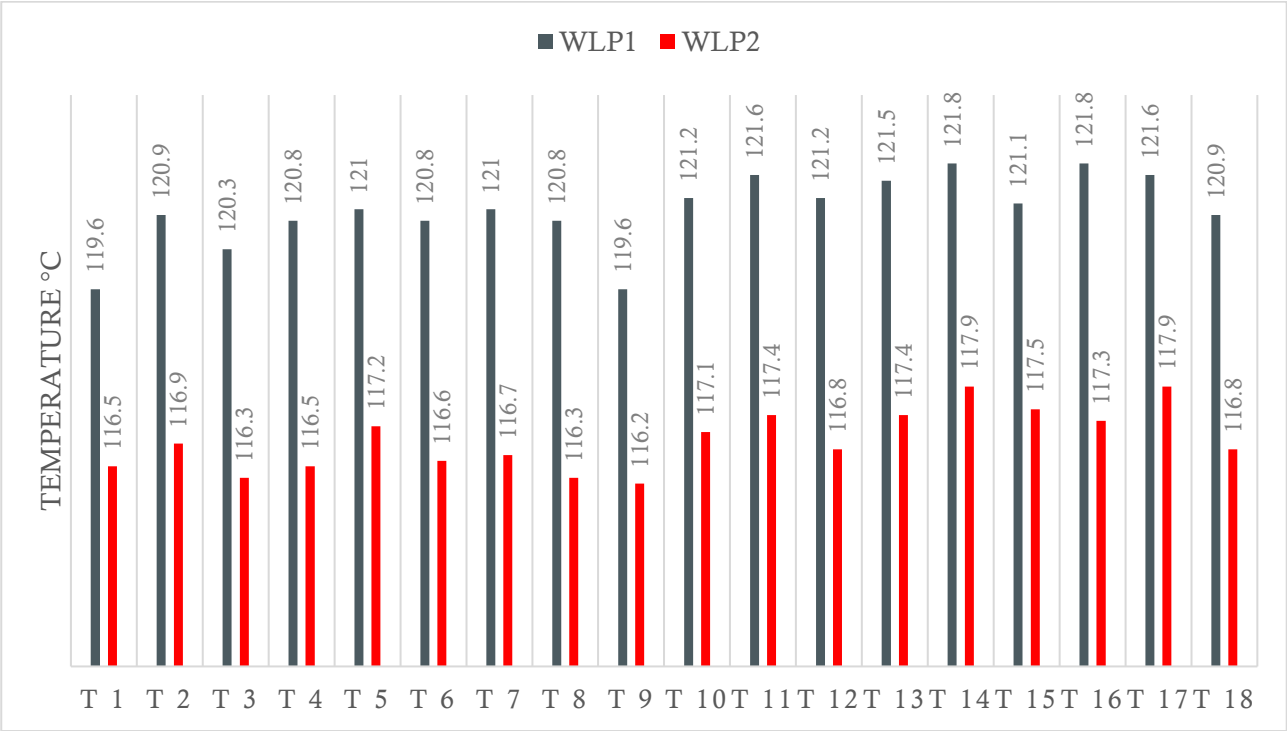

Figure 19: Comparison of the average temperature between a power hybrid with WLP1 and WLP2

The simulation results show that it would be recommended to use the better thermal paste (WLP2). Both hotspot temperature and average chip temperature could be decreased by approximately 4 °C.

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2.5.2 Heat sink material

Furthermore copper instead of aluminium as heat sink material was investigated. Because copper has 1.8 times the thermal conductivity of aluminium, a heat sink made out of copper should perform far better.

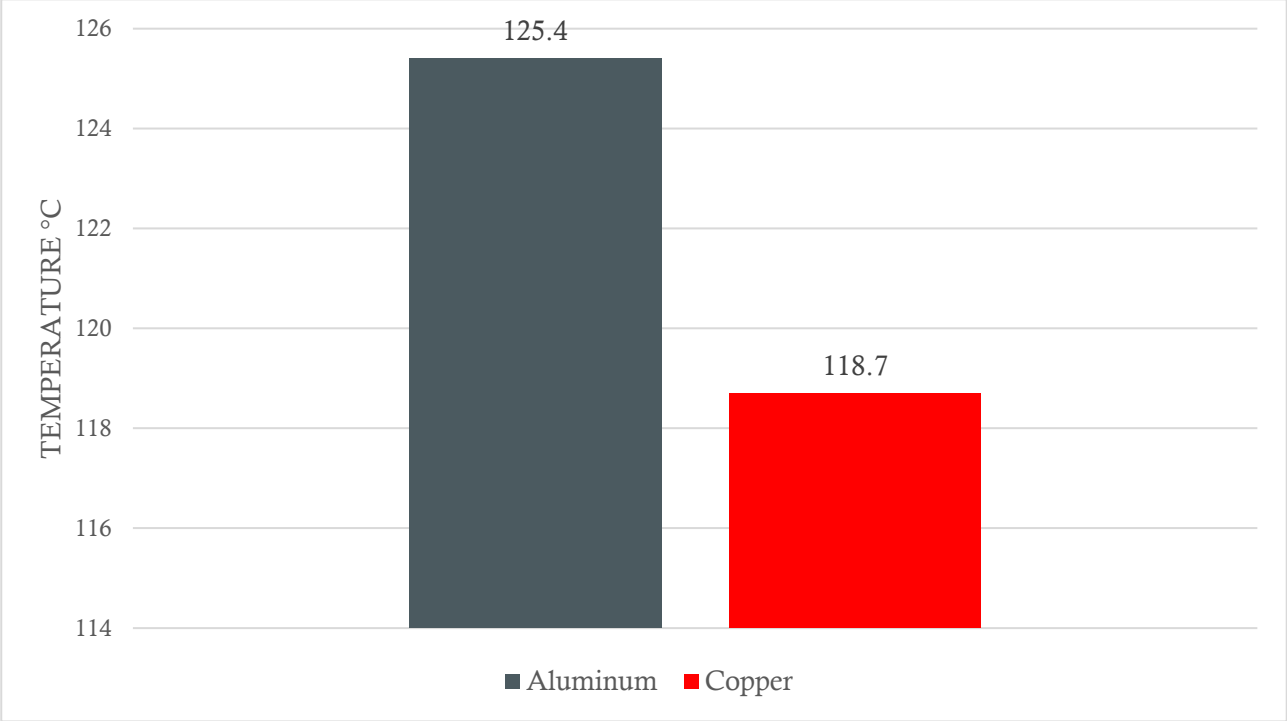

Figure 20: Comparison of the hotspot temperature of a copper and an aluminium heat sink

Figure 21: Comparison of the average chip temperature of a copper and an aluminium heat sink

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As expected the simulation results in figures 20 and 21 show that the copper heat sink performs far better than the aluminum heat sink. The hotspot temperature and the average chip temperature decrease by 6.7 °C. A reduction of the temperature in a single digit range increases the lifetime and current carrying capacity of the chips. Because silicon carbide chips are very expensive, this justifies the use of copper as heat sink material. Because the highest temperature gradients are located next to the power hybrids it is not necessary to have a full copper heat sink. Instead a copper plate with copper pins was used as the heat sink for the power hybrids. The case with the fluid channels and the inlet and outlet will still be made out of aluminum.

2.6 Fourth iteration: Nearly finalized version

The CAD model of the nearly finalized version of the module and heat sink (version 4) are pictured in figure 22.

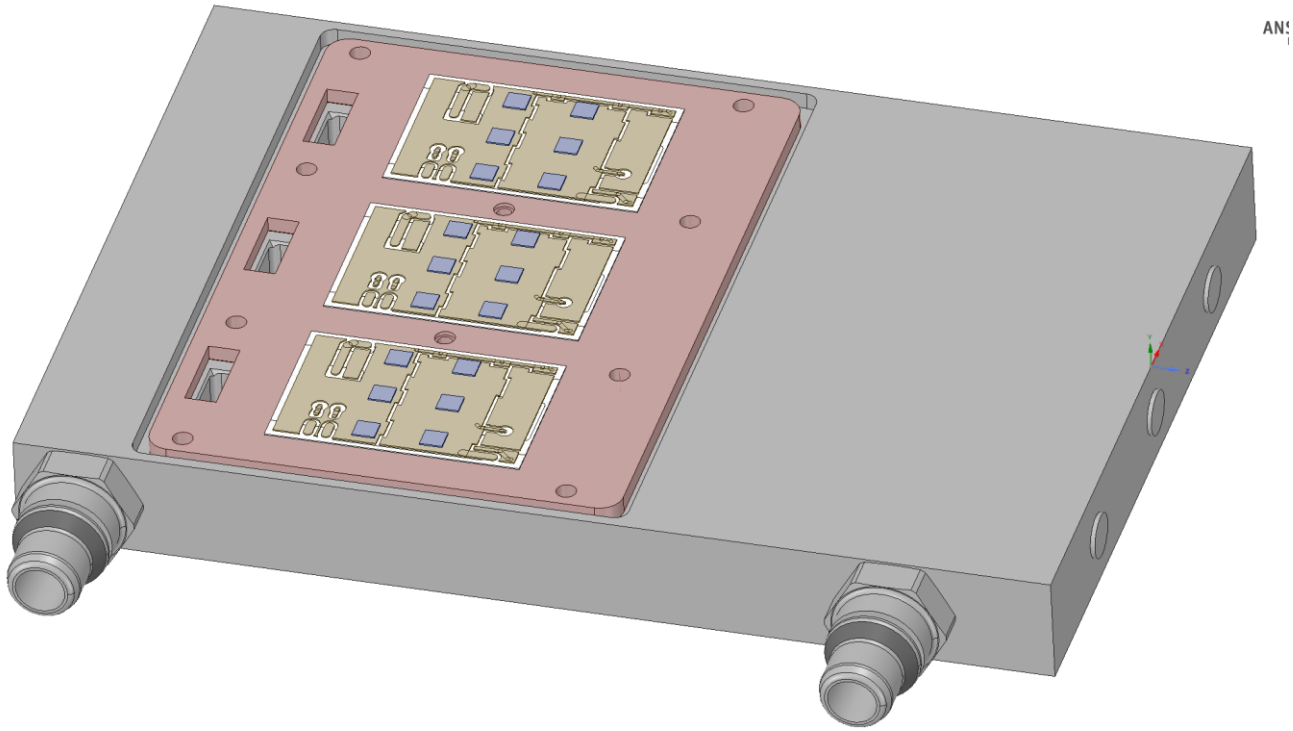

Figure 22: CAD model of version 4

Version 4 has the following properties:

- chip distance of 8 mm
- construction with 3 power hybrids
- an optimized Heat sink containing of:
  - A copper plate and pins beneath the power hybrids
  - An aluminium body
  - Pin fins
  - Optimized Fluid flow beneath the 3 Modules
  - Pressure drop of 200 to 250 mbar

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- Because of the length requirements defined by the motor size the inlet and outlet had to be located at the side of the heat sink.

2.6.1 Optimization of the nearly finalized heat sink

It was decided to use a pin fin type heat sink because of the better manufacturability. It is possible to investigate the performance of different types of fins (e.g. oval, square…) in the future. Originally the inlet and the outlet were located in the middle of the narrow end the heat sink body. But because of the electrical motor requirements the inlet and outlet had to be located at the side of the heat sink. The most important goal was to achieve a certain fluid flow beneath the 3 modules. In previous simulations the chips of the middle phase get hotter than the ones at the sides. To cool all three Phases properly the volumetric flow beneath the middle module should be higher than beneath the modules on the side.
In order to achieve the desired volume flow distribution various different heat sink versions were constructed and simulated. Of the various variants, those were selected where the temperatures of the individual modules were as low as possible and the temperature difference was as low as possible too. At last the heat sink pictured in figure 22 was chosen.

2.6.2 Fluid flow simulations

To verify the achievement of the goal of the volumetric flow under the modules in subchapter 1 a fluid flow simulation was performed. In figure 23 one can see the extracted fluid volume from the heat sink.

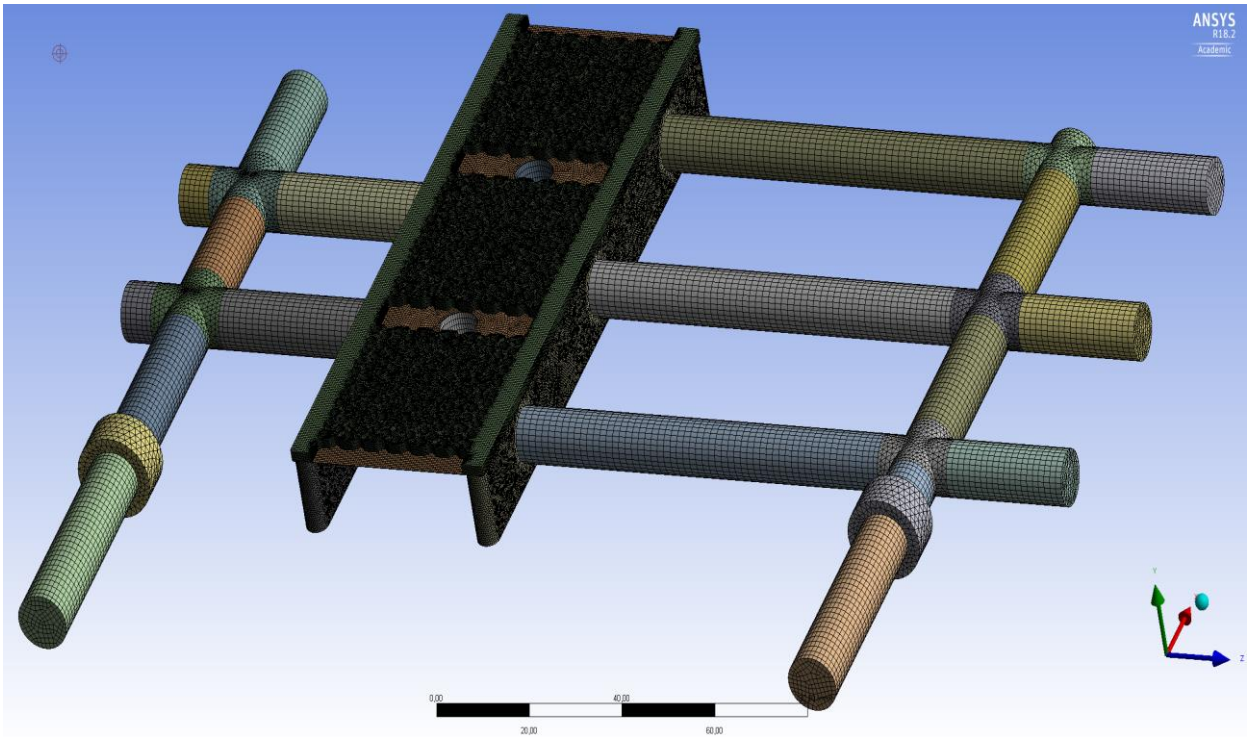

Figure 23: Mesh of the fluid volume

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Table 1: Volumetric flow through the heat sink

Volumetric Flow [L/min]							
E1	E2	M1	M2	M3	A1	A2	A3
4.29	5.7	3.18	3.54	3.27	4.61	2.88	2.51

Table 1 shows the results of the simulation. E1 and E2 are the two channels on the inlet side. One can see that the volumetric is relatively balanced, with E2 carrying slightly more liquid. M1 to M3 are the fluid sections under the corresponding module. As desired the results show that the volumetric flow under the middle module M2 is higher than under the modules M1 and M3. On the outlet side A1, A2 and A3 have different levels of volumetric flow with A3 carrying significantly more liquid. This point is not problematic as no large temperature gradients are expected in this area.

2.6.3 Thermal simulations

Final a thermal simulation to investigate the thermal behavior of the nearly finalized version was performed. The boundary conditions of the simulation were defined in chapter 2. In figure 24 the contour plot of the result is shown.

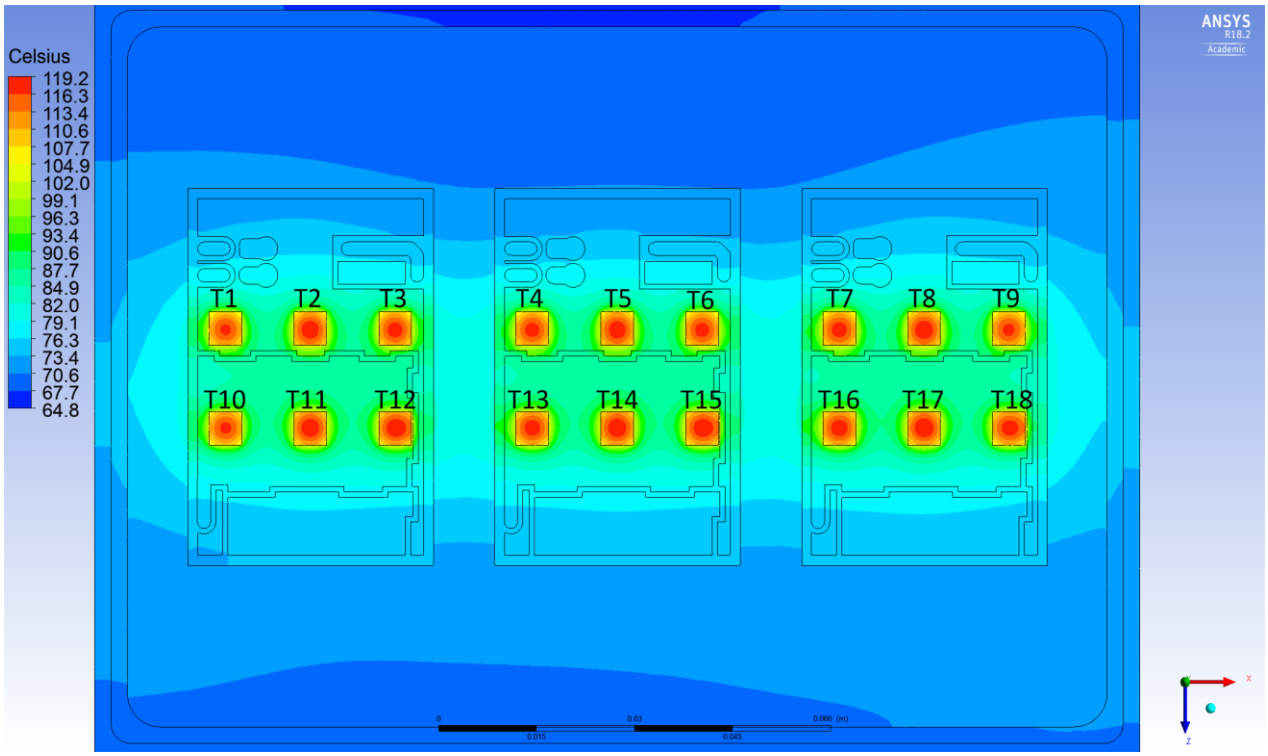

Figure 24: Thermal contour of the power hybrid of version 4

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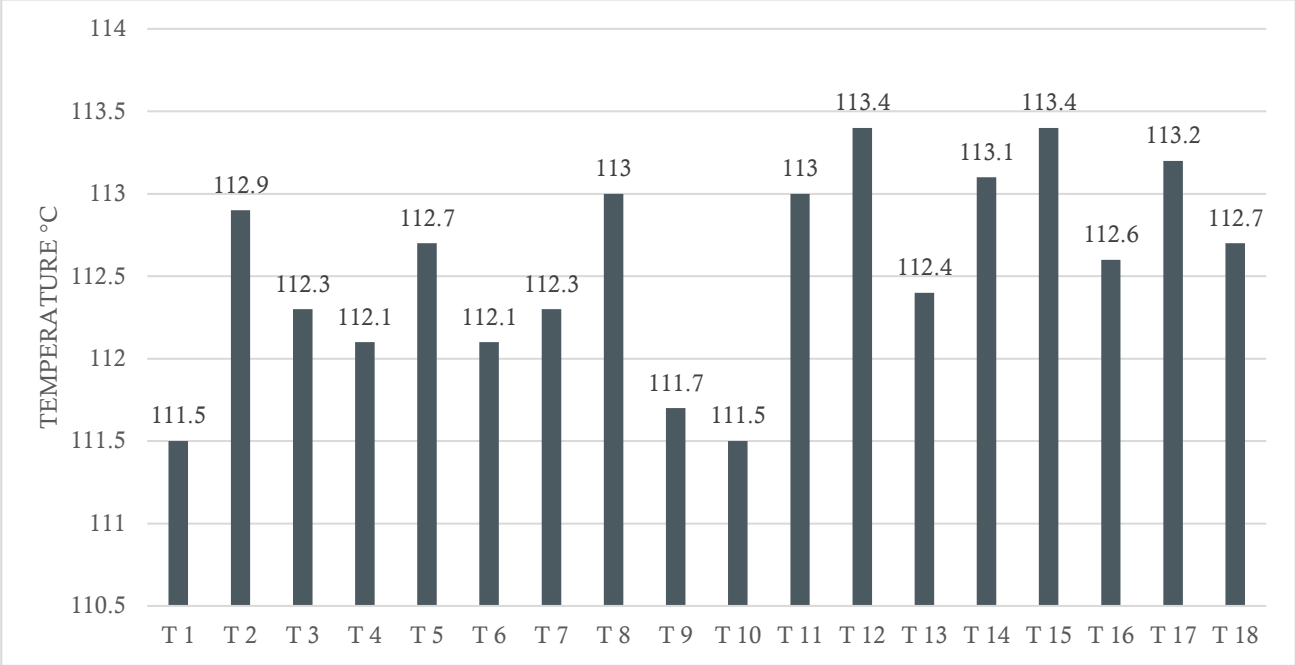

Figure 25: Average chip temperatures of version 4

The temperature of the hotspot is 119.2 °C. This is around 1 °C higher than the hotspot in the previous simulation with a copper heat sink in chapter 2. In the bar chart in figure 26 one can see the corresponding average chip temperatures. The chips T1 and T10 are far cooler than the others. One assumption is that these two chips are located at the edges and have a relative large copper area around them. The chips on the other side like T18 are located at the edge too. But probably because of their location at a copper edge their average temperature becomes higher. In further studies the optimized placing of the chips will be investigated.

The bar chart in figure 27 shows a comparison of the average chip temperature between version 3 with copper heat sink and version 4. On the average the temperatures of the recent version are 1 °C higher than in the previous simulation. The reason for this is that in the preceding simulation the copper on the top side of the power hybrid was unstructured and functioned well as a heat spreader.

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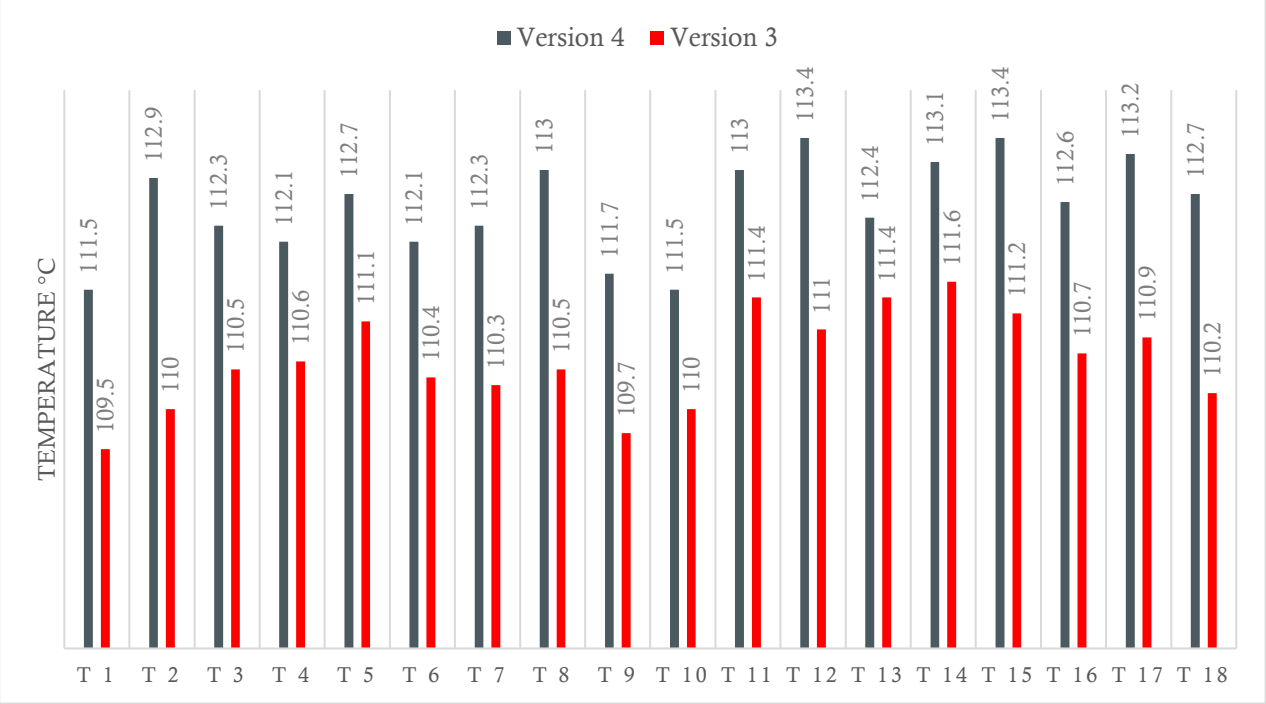

Figure 26: Comparison of the average chip temperatures of version 4 and 3

2.7 Conclusion

The thermal performance of the inverter was significantly improved with the optimizations presented in this report. Especially the chip distance has proven to be the best option to reduce the overall temperature and temperature difference of the chips. Because of the reduced temperature the current yield of the SiC chips could be improved. As SiC chips are very expensive it is worthwhile to increase the area of the substrate. The same considerations apply to the use of a copper heat sink.

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3. Summary

This report describes the various simulation and optimization steps of the inverter in WP 4. At the beginning a design idea optimized with regard to packing density is analyzed for possible improvements. Subsequently, a number of possible optimizations were considered, with the chip spacing proving to be the best approach. Using various test structures, the thermal influence of the chip spacing was investigated and optimized for the requirements of the inverter. In addition alternative materials for the use as heat sink and heat conducting paste were investigated. Finally design variations of the heat sink with an early design of the power hybrids are investigated and optimized in terms of thermal performance and fluid dynamics. In the project, it is also planned to further investigate individual variants not selected for the prototype.

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4. References

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