DRIVEMODE

Integrated Modular Distributed Drivetrain for Electric & Hybrid Vehicles

Document title: Simulation Report

D4.5: Report 2 with simulation and measurement results
WP 4, T 4.4

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DRIVEMODE

Technical references

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* PU = Public

PP = Restricted to other programme participants (including the Commission Services)

RE = Restricted to a group specified by the consortium (including the Commission Services)

CO = Confidential, only for members of the consortium (including the Commission Services)

v	Date	Comment	Author	Beneficiary
0.1	07/10/2019	Initial draft	Nathalie Becker	TUI
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Executive Summary

This report summarizes the thermal simulations, fluid simulations and corresponding optimizations done for the converter. The report explains the optimization process of the converter starting from the previous report to the design freeze version. A thermal characterization was done to investigate the temperature dependent behaviour of the presented inverter and to find further possible improvements. In addition, a comparison between an originally planned version of the inverter with 4 chips and the presented inverter was conducted to examine the effectiveness of the performed optimizations. Finally, the influence and thermal interaction between the chips and the flex-layer contacting the chips was studied.

The simulations were done in the DRIVEMODE work package 4 (WP 4), Converter, task 4.4, Modelling and simulation.

Attainment of the objectives and if applicable, explanation of deviations

This report is a summary of performed simulations and optimizations in regard of thermal performance and fluidic flow for the converter in WP4. It contains the individual steps of the thermal and fluidic optimization process starting from the last report (deliverable 4.2) up to the design freeze inverter. The measurements of the inverter could not be performed at this point due to a delay in the manufacturing. The measurement results will be included in the final report.

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Nomenclature

SiC	Silicon Carbide
Version 3	Inverter version before version 4 from the previous report D4.2
Version 4	Last inverter version of the previous report D4.2
Power Hybrid	Assembled AMB substrates
AMB	Active Metal Bonding

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1. Introduction

1.1 Introduction Drivemode

DRIVEMODE is a project funded by the European Commission under the Horizon 2020 framework. The project aims at designing a compact modular integrated drive module (IDM) for pure electric vehicles (PEVs) and hybrid electric vehicles (HEVs).
The IDM developed in the DRIVEMODE project will be a drivetrain platform that then can be adopted depending on the application e.g. demonstration vehicle. The modularity and scalability of the IDM will be used to support a wider range of application. This document will
Report on the thermal and fluid simulations performed for the converter including corresponding optimizations with regard to thermal performance.

1.2 Scope of document

This report is a summary of the finished thermal and fluid simulations for the converter as well as a summary of several design iterations to optimize the thermal behaviour.

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2. Thermal and fluid simulations

2.1 Simulation conditions

The simulations presented in this report were performed under the following conditions:

- Power dissipation per chip: 137 W
- Current per phase: 140 A
- Cooling fluid temperature at the inlet: 65°C
- Flow rate: 10 L/min
- Consideration of thermal paste and sinter paste
- Ambient pressure: 1.01325 bar
- Interface wall between fluid and solid: smooth wall
- Turbulence of the fluid: Laminar flow

These conditions were defined and agreed together with the project partners. The power dissipation of 137 W per chip was simulated with ANSYS Fluent and the current of 140 A_{rms} per phase. The CAD models of the converter and the heat sink were constructed in SolidWorks. The thermal and fluid simulations were performed in the ANSYS Workbench environment. A schematic drawing of the simulation model is pictured in figure 1.

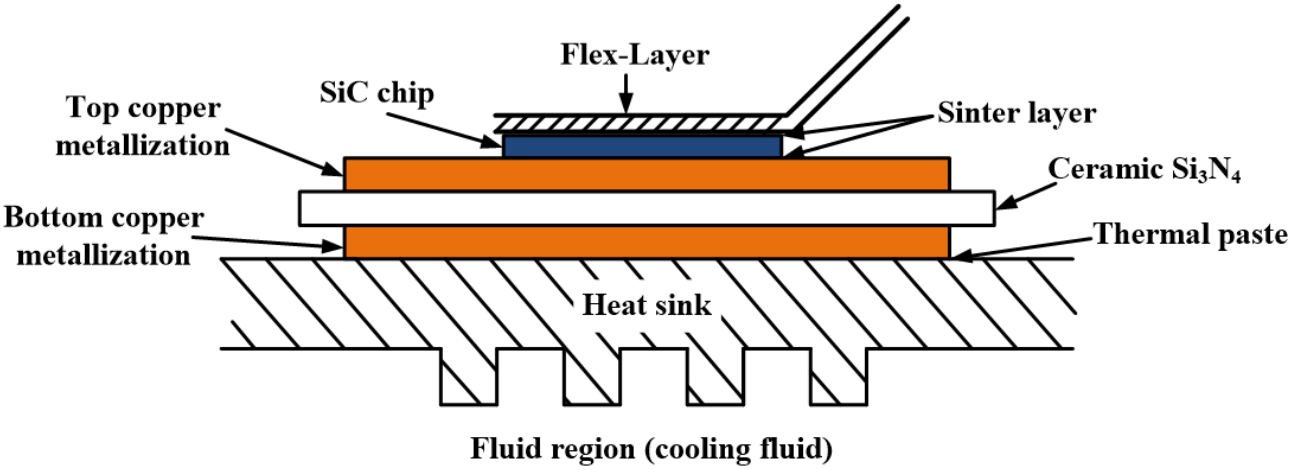

Figure 1: Schematic of the simulation model

The inverter is simulated by means of a FEM simulation. The simulations performed were steady state thermal simulations coupled with fluid dynamic simulations. This was done to properly simulate the heat conduction coefficient at the interface of the fluid and solid region. Coupled heat conduction takes place at the interfaces of the solid bodies. Additionally, at the interface between SiC chip and upper copper metallization sinter paste is assumed as 2D material (fig. 1). Located at the interface between lower copper metallization and heat sink is heat conducting paste as 2D material (fig. 1). The flow of the coolant through the heat sink is calculated using the Shear stress transport model.

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2.2 Further optimizations

In the previous report the latest design stage (version 4) had still some potential for further optimizations. These simulations were performed with the 80 W power dissipation used in the previous report for better comparability. The issue was that the overall chip temperatures were 1 °C above the chip temperatures in the previous version (version 3). Especially the chips T12, T15 and T18 became noticeably hotter compared to version 3. Whereas the chips T1, T9 and T10 were cooler despite their position on the edges. The assumption was that the structuring of the top copper metallization and the placement of the chips are the reason for this temperature distribution. T12, T15 and T18 were located closely to a copper edge and T1, T9 and T10 had more copper and less heat sources surrounding them compared to the other chips (see fig 2). Because of this a test simulation was done to investigate the influence of the chip placement and the copper trenches. All chips were shifted, so the distance between the copper edge and the outer chips were equal at both sides (see fig. 3). The results of this simulation and a comparison to the version without shifted chips are depicted in figure 2 to 4.

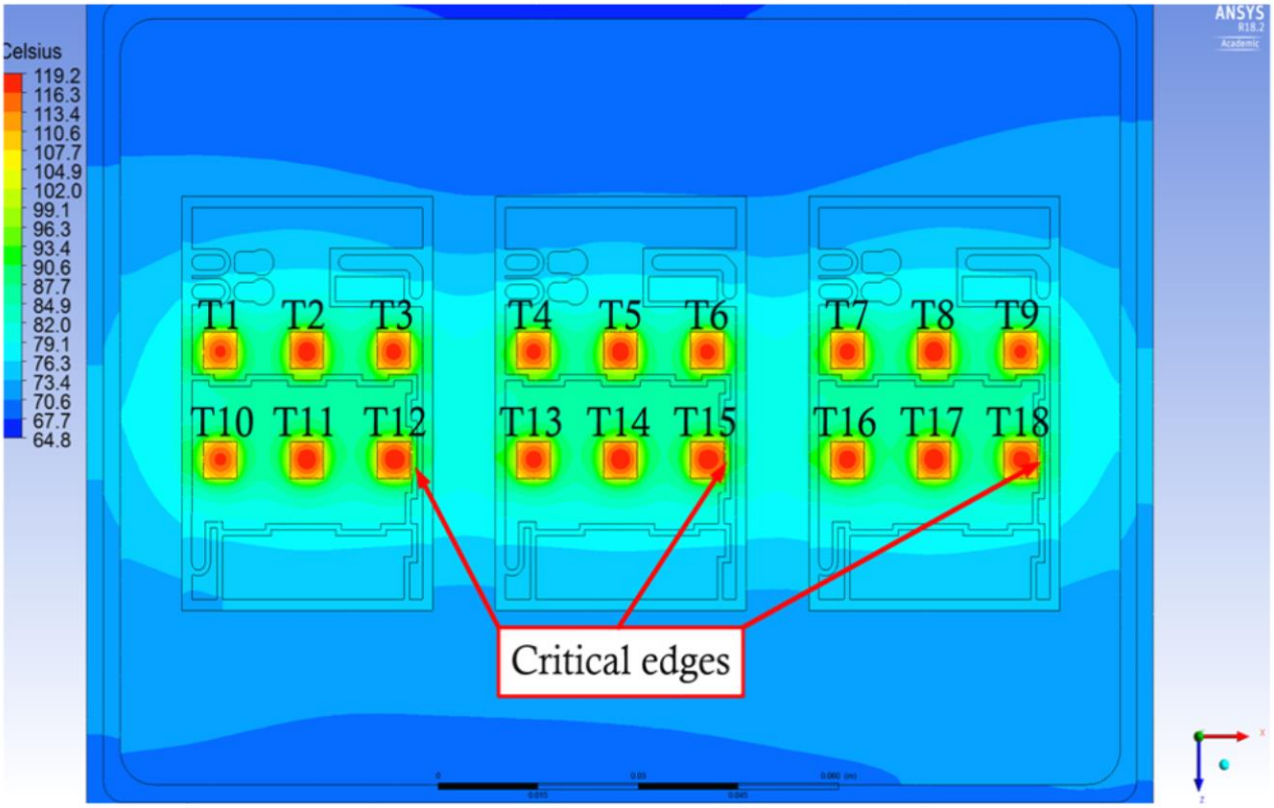

Figure 2: Thermal contour plot of the inverter before the chip shifting

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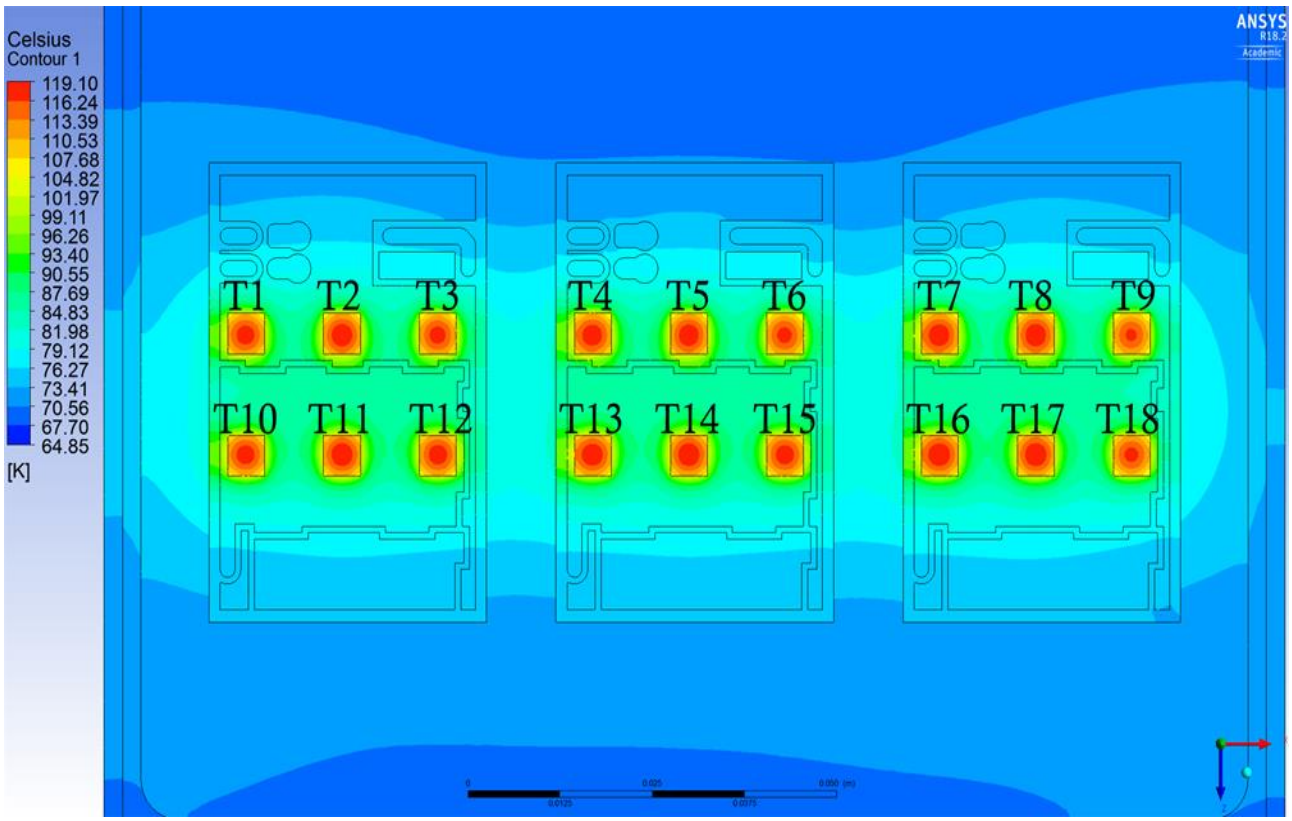

Figure 3: Thermal contour plot of the inverter after the chip shifting

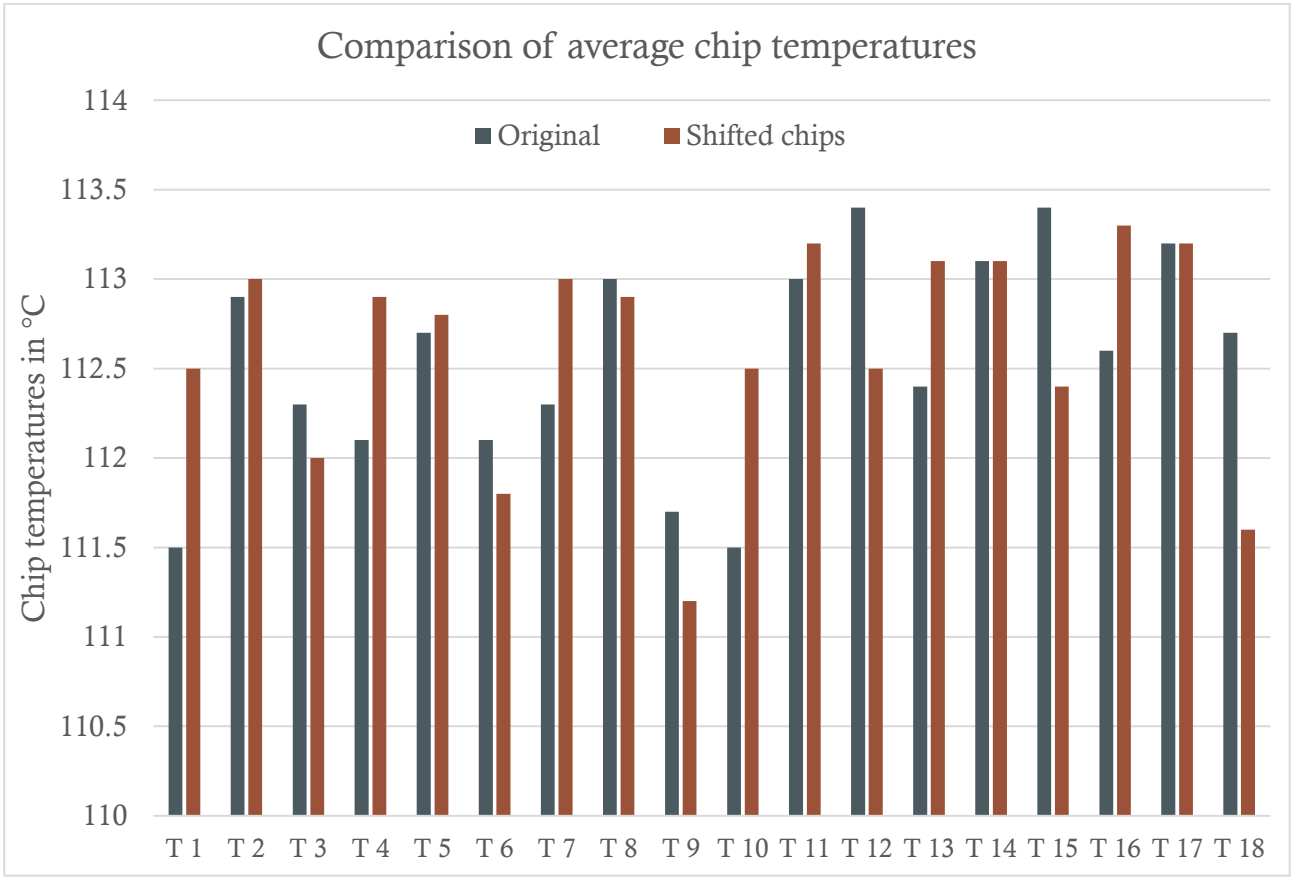

Figure 4: comparison of the average chip temperatures

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The graph shows that the shifting of the chips doesn't achieve the desired results. The desired result was a better uniformity of the chip temperatures. Instead the temperature difference between the hottest and coolest chips increased from 1.9 °C to 2.1 °C. The aforementioned "critical" chips show a seemingly random temperature alteration. It was expected to decrease the temperature of T12, T15 and T18 and increase the temperature of T1, T9 and T10. One possibility for this effect is the placing of the chips above the pin structure of the heat sink. The pin structure was not shifted with the chips and as a result the relative overlap between chips and pins changed. So, it was decided to do a full redesign of the power hybrids with less copper trenches for better heat spreading and an adapted pin structure.

2.3 Thermal characterization

The temperature dependent behaviour of the inverter was investigated. The inverter version used was the not redesigned version from 2.1 (version 4). The investigation was performed by variation of the volume flow and the inlet temperature. Table 1 lists the boundary condition for the performed simulations.

Current value	Variable	Start	End	Step size
140 A	Volume flow	10 l/min	1 l/min	1 l/min
	Inlet temperature	65 °C	40 °C	1 °C
70 A	Volume flow	10 l/min	4 l/min	2 l/min
	Inlet temperature	65 °C	50 °C	5 °C
35 A	Volume flow	10 l/min	4 l/min	2 l/min
	Inlet temperature	65 °C	50 °C	5 °C

Table 1: Simulation boundary conditions

The simulation was done under variation of the parameters mentioned in table 1. 140 A is the max RMS current for the inverter for each phase. The volume flow of 10 l/min is the recommended value to guarantee the best cooling and 1 l/min is a total failure of the cooling circuit. The inlet temperature of 65 °C is the worst case temperature and 40 °C is the temperature for better cooling conditions. The simulations were repeated with lower currents to simulate average load conditions (70 A) and low load condition (35 A). The step size was increased for these to reduce the simulation time and the missing steps were approached by interpolation. These values were agreed together with the partners.
For following simulations the temperature dependent power loss of the SiC chips was taken into account. This was done via User Defined Function in ANSYS Fluent which describes the temperature dependent power loss of the SiC MOSFETs and was created with aid of a device simulation program. Figures 5 to 7 show the results of the parameter variation.

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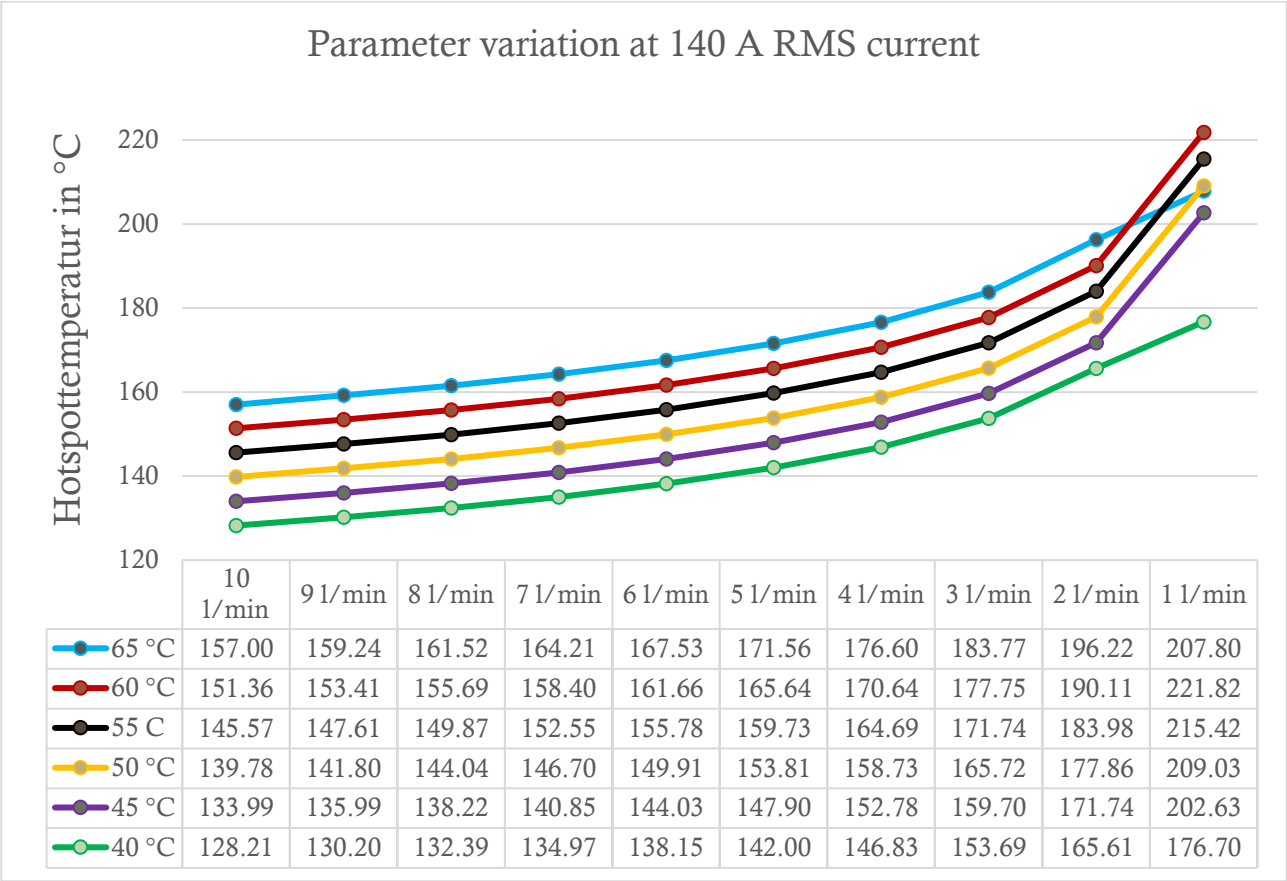
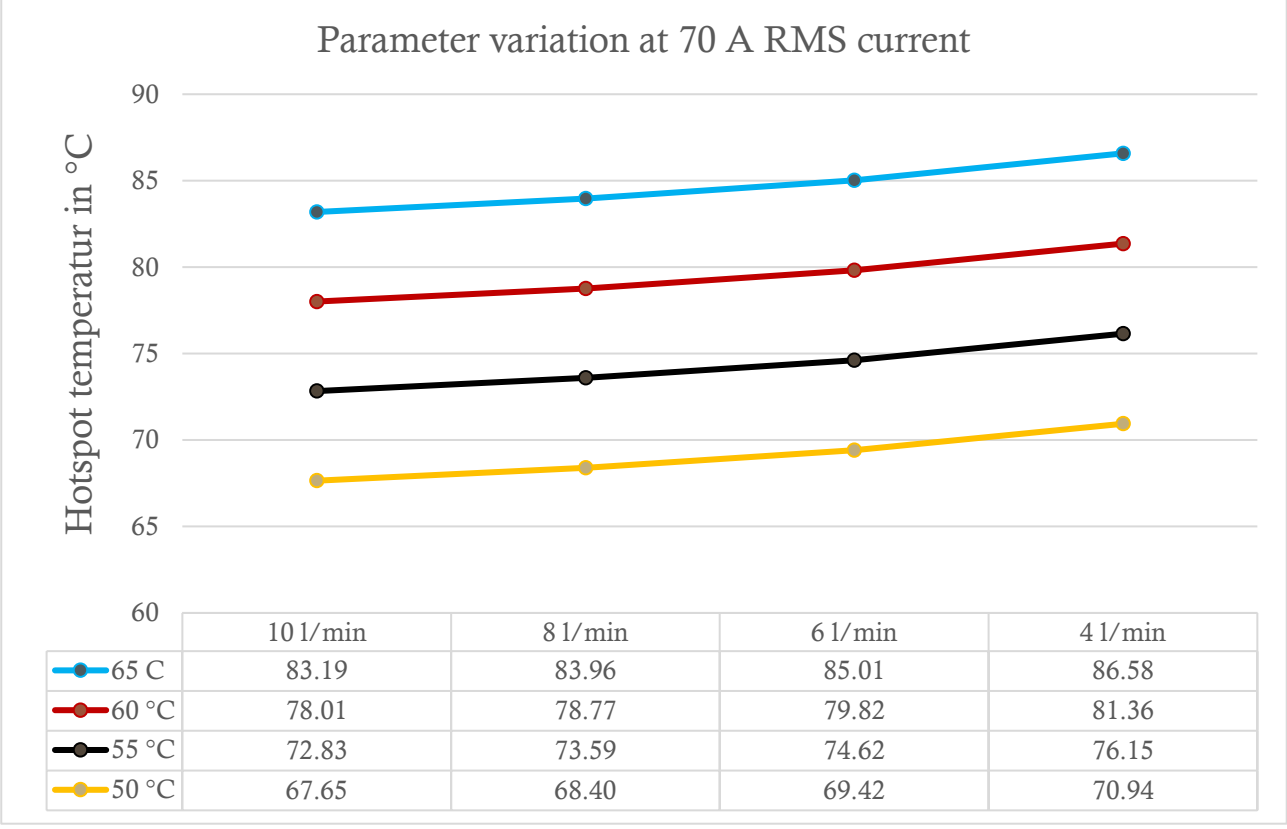


	10 l/min	9 l/min	8 l/min	7 l/min	6 l/min	5 l/min	4 l/min	3 l/min	2 l/min	1 l/min
65 °C	157.00	159.24	161.52	164.21	167.53	171.56	176.60	183.77	196.22	207.80
60 °C	151.36	153.41	155.69	158.40	161.66	165.64	170.64	177.75	190.11	221.82
55 C	145.57	147.61	149.87	152.55	155.78	159.73	164.69	171.74	183.98	215.42
50 °C	139.78	141.80	144.04	146.70	149.91	153.81	158.73	165.72	177.86	209.03
45 °C	133.99	135.99	138.22	140.85	144.03	147.90	152.78	159.70	171.74	202.63
40 °C	128.21	130.20	132.39	134.97	138.15	142.00	146.83	153.69	165.61	176.70

Figure 5: Results of the parameter variation at 140 A RMS current



	10 l/min	8 l/min	6 l/min	4 l/min
65 C	83.19	83.96	85.01	86.58
60 °C	78.01	78.77	79.82	81.36
55 °C	72.83	73.59	74.62	76.15
50 °C	67.65	68.40	69.42	70.94

Figure 6: Results of the parameter variation at 70 A RMS current

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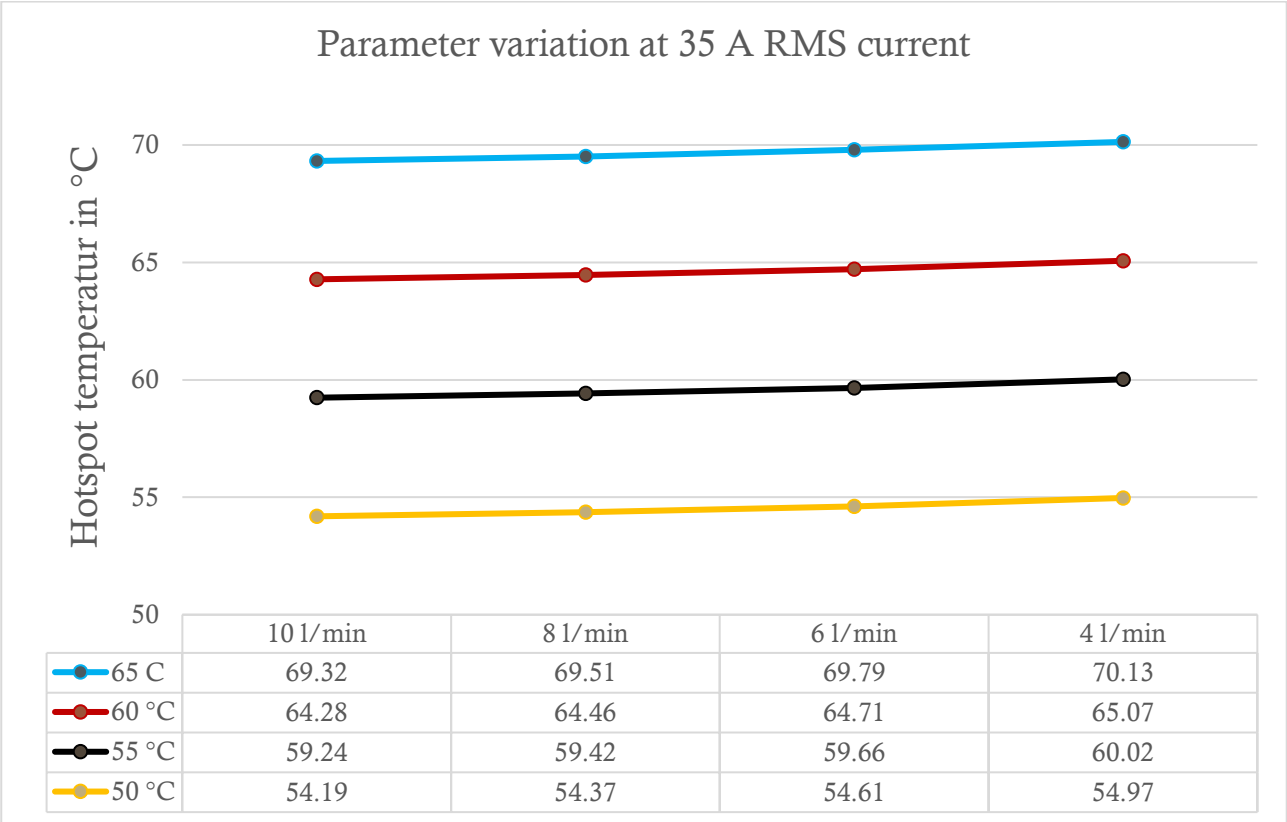

	10 l/min	8 l/min	6 l/min	4 l/min
65 C	69.32	69.51	69.79	70.13
60 °C	64.28	64.46	64.71	65.07
55 °C	59.24	59.42	59.66	60.02
50 °C	54.19	54.37	54.61	54.97

Figure 7: Results of the parameter variation at 35 A RMS current

The results in figure 5 to 7 demonstrate that the inlet temperature has a great influence on the chip temperatures. The lower the inlet temperature the better the thermal performance of the inverter and vice versa. Therefore, the performance of the higher level cooling system directly influences the performance of the inverter. For every 1 °C increase of the inlet temperature the hotspot temperature (limiting factor) increases by 1.2 °C. The volume flow has a great influence too. As expected, the lower the volume flow the hotter the chips become this dependence is non-linear and escalates down from 4 l/min (see fig. 5). If the inlet temperature rises, the volume flow must be increased accordingly to prevent damage to the chips. To ensure the best cooling capability it is recommended to keep the volume flow at 10 l/min at all times. With lower inlet temperatures it is possible to reduce the volume flow. But the delta temperatures during load cycles must be considered because these reduce the lifetime of the chips.
The simulation results show that a better performance of the higher level cooling system can significantly enhance the thermal performance of the inverter. Therefore, improvement of lifetime and reliability or a higher current carrying capacity are possible. The potential of a higher current by reducing the inlet temperatures can be investigated in the future.

2.4 Final design

One goal of the redesign was to reduce the amount of copper trenches of the copper metallization around the chips to increase the area for heat spreading. This was done by shifting most the structuring for the current path into the flex layer. Figures 8 to 9 show the previous version and the redesigned power hybrids. In the redesign (fig. 9) the edges around the chip were removed and the chips have now more copper surrounding them for heat spreading purpose. Only the

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TOP chips (lower chips row in fig. 9) are still very close to the copper trench but due to manufacturability was not possible to shift them further away.

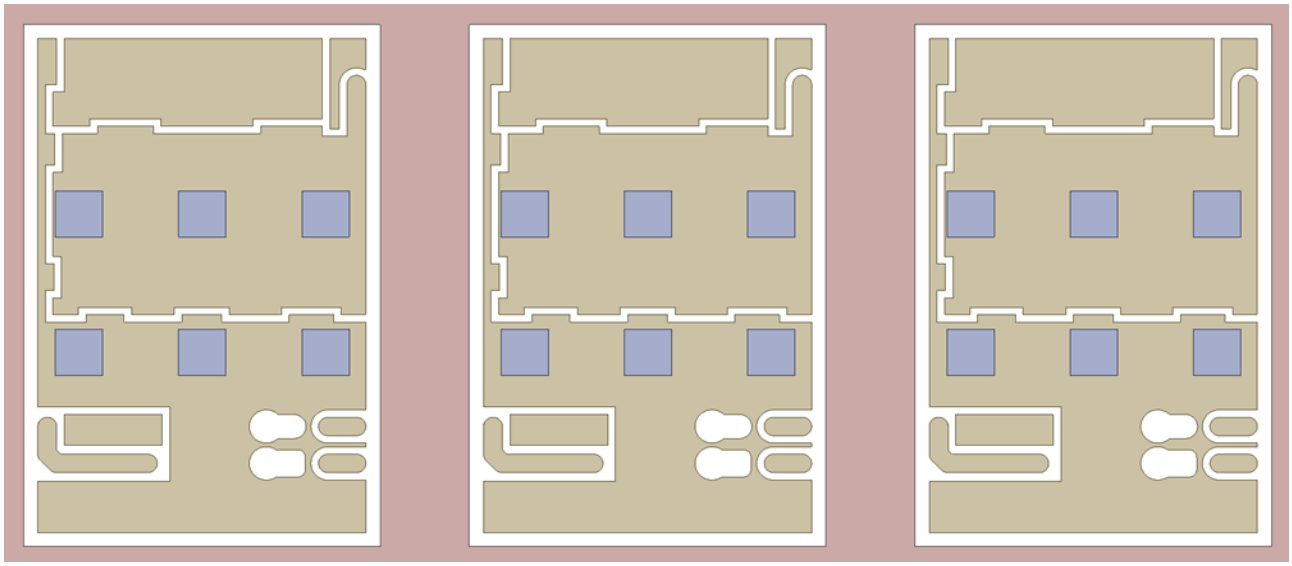

Figure 8: Power hybrids before redesign

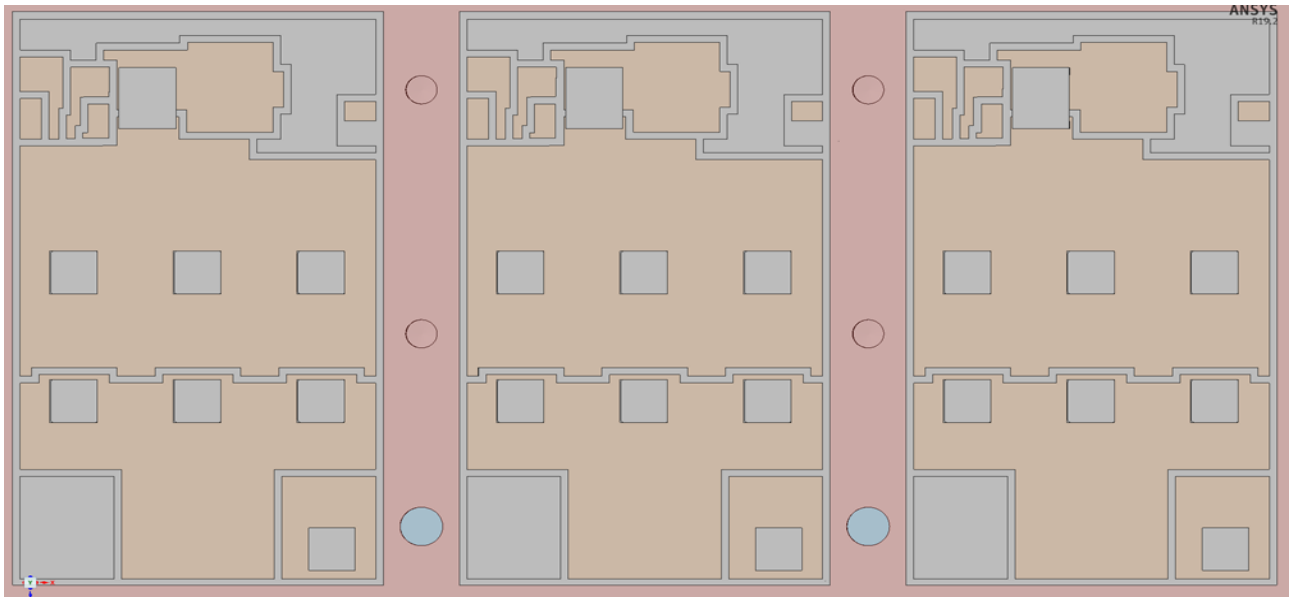

Figure 9: Power hybrids after redesign

Figure 10 depicts the simulation result of the redesigned power hybrid. Because the TOP chips (lower chip row in fig. 9) are still very close to the copper trench these chips become hotter than the BOT chips (top row in fig. 9) by approximately 3 °C. This is in addition to the heating of 2 °C by the cooling fluid. With the exception of the temperature difference between the TOP and BOT chips, the relocation of the copper trenches produced a good result. The chip temperatures are more uniform compared to the previous version (see. fig. 3). Apart from the elevated temperature of the TOP chips, the overall temperatures are good. The hotspot temperature is 154.47 °C (see fig. 10) and the average temperatures of the chips are around 143 °C (see fig. 11). These temperatures are well lower than the max allowed temperature of 170 °C for the chips.

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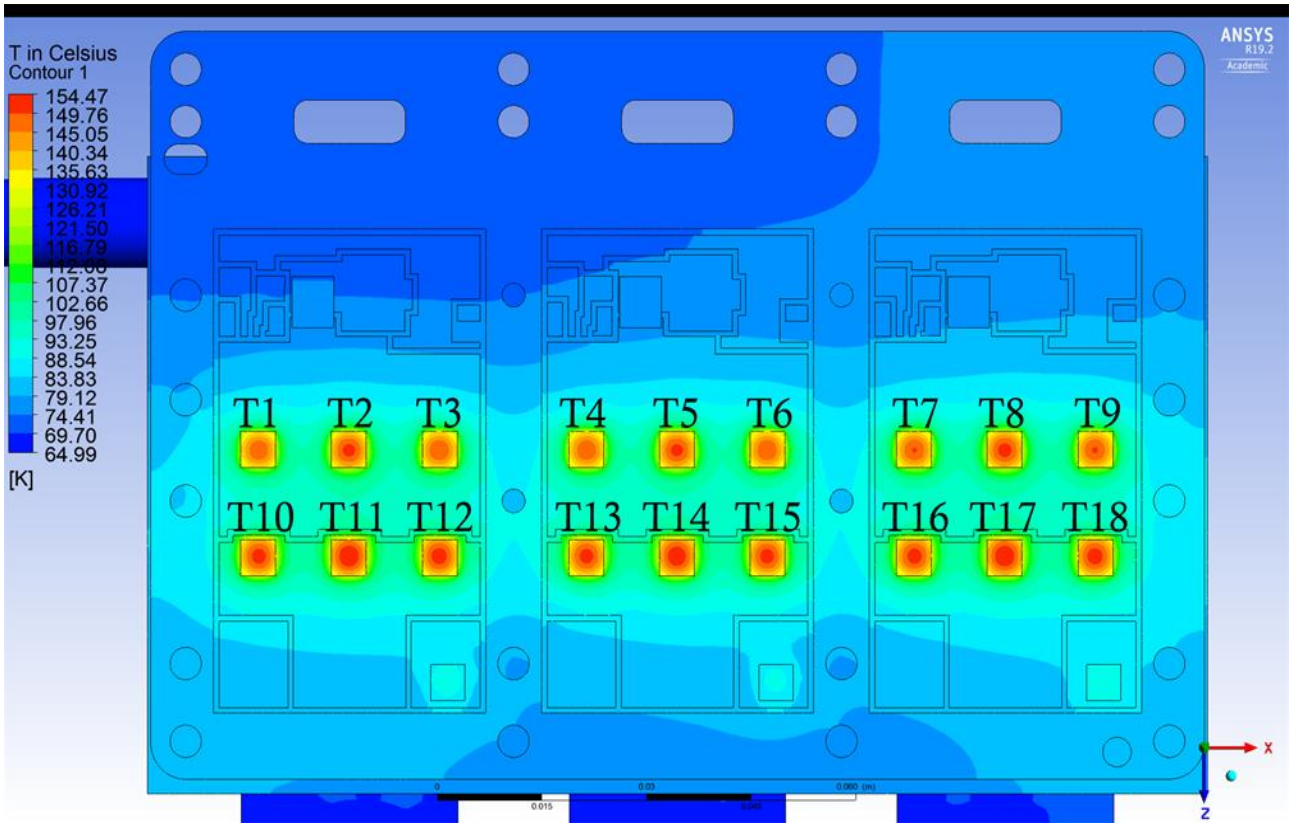

Figure 10: Thermal contour plot of the redesigned power hybrid

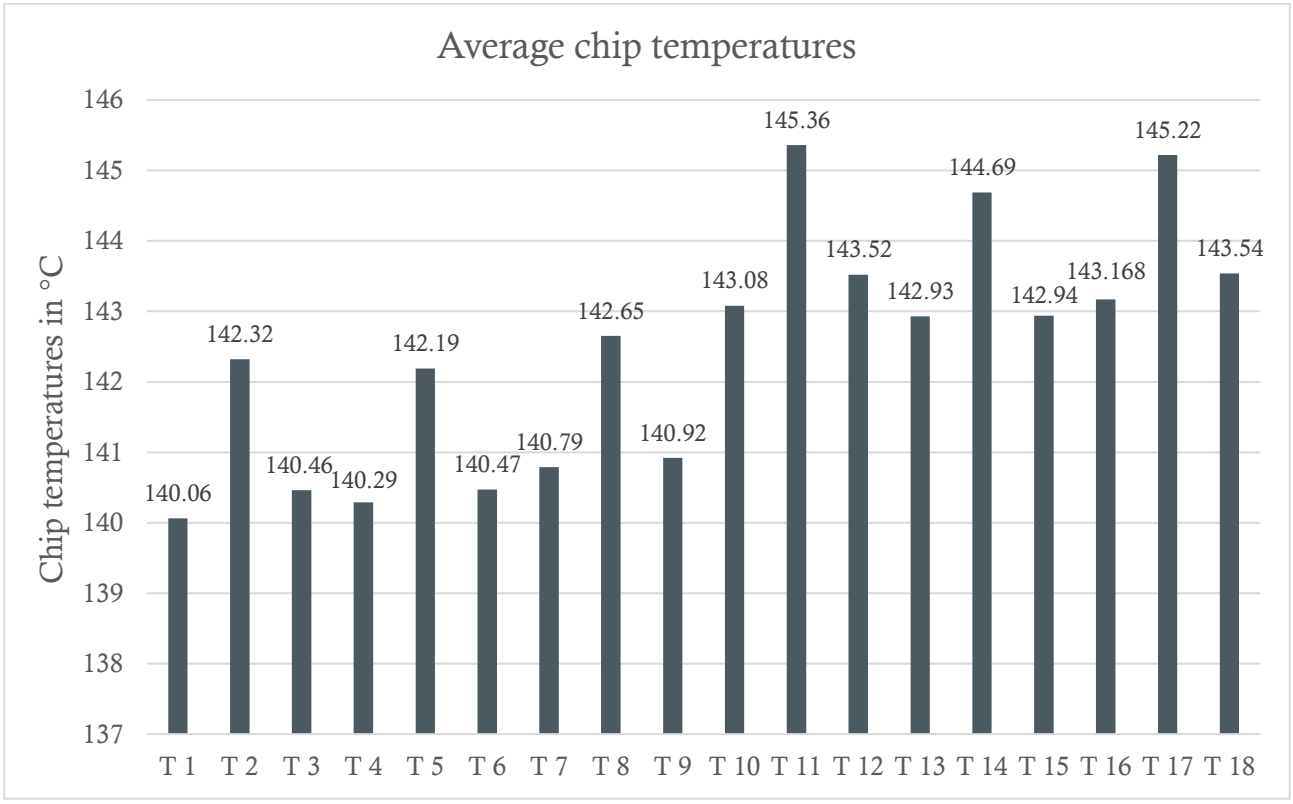

Figure 11: Graph of the average chip temperatures of the redesign

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The second goal of the redesign was to further improve the fluid flow beneath the power hybrids. The channel in the heat sink were completely redesigned in two steps. Figure 12 and 13 depict the original version and the redesigned version. Instead of round drilled channels there are now flat milled channels. This has two advantages:

1. the flat milled channels allow for a flatter heat sink and reduce the overall height of the inverter
2. the increased cross section of the channels reduces the pressure drop in the channels

Furthermore, the pin structure was reworked and the pressure drop was increased from 127.3 mbar to 194 mbar. This serves to improve the cooling performance of the heat sink. The volume flow distribution beneath the modules remained the same. The second design iteration was necessary because of a vortex in front of the pin region that produced an unnecessary pressure drop. Without this vortex the overall pressure drop was reduced from 208.8 mbar to 176 mbar.

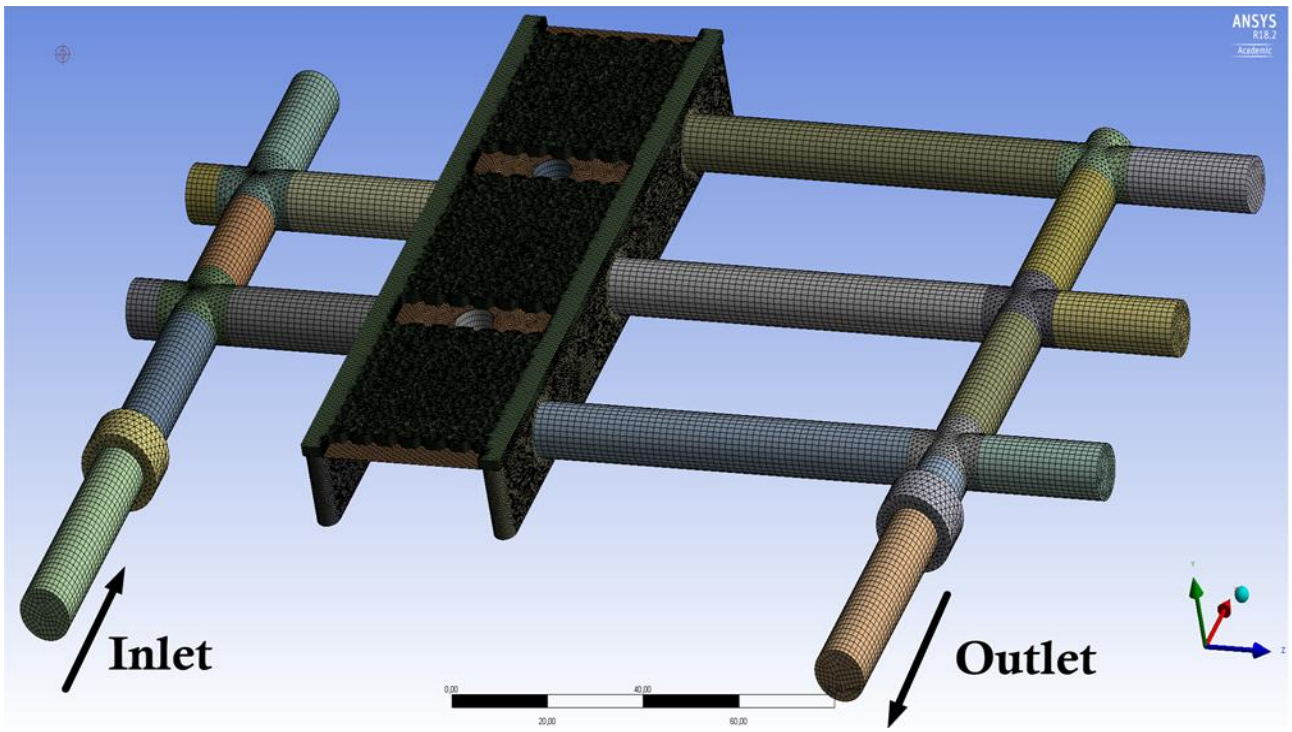

Figure 12: Version 4 fluid region of the previous report

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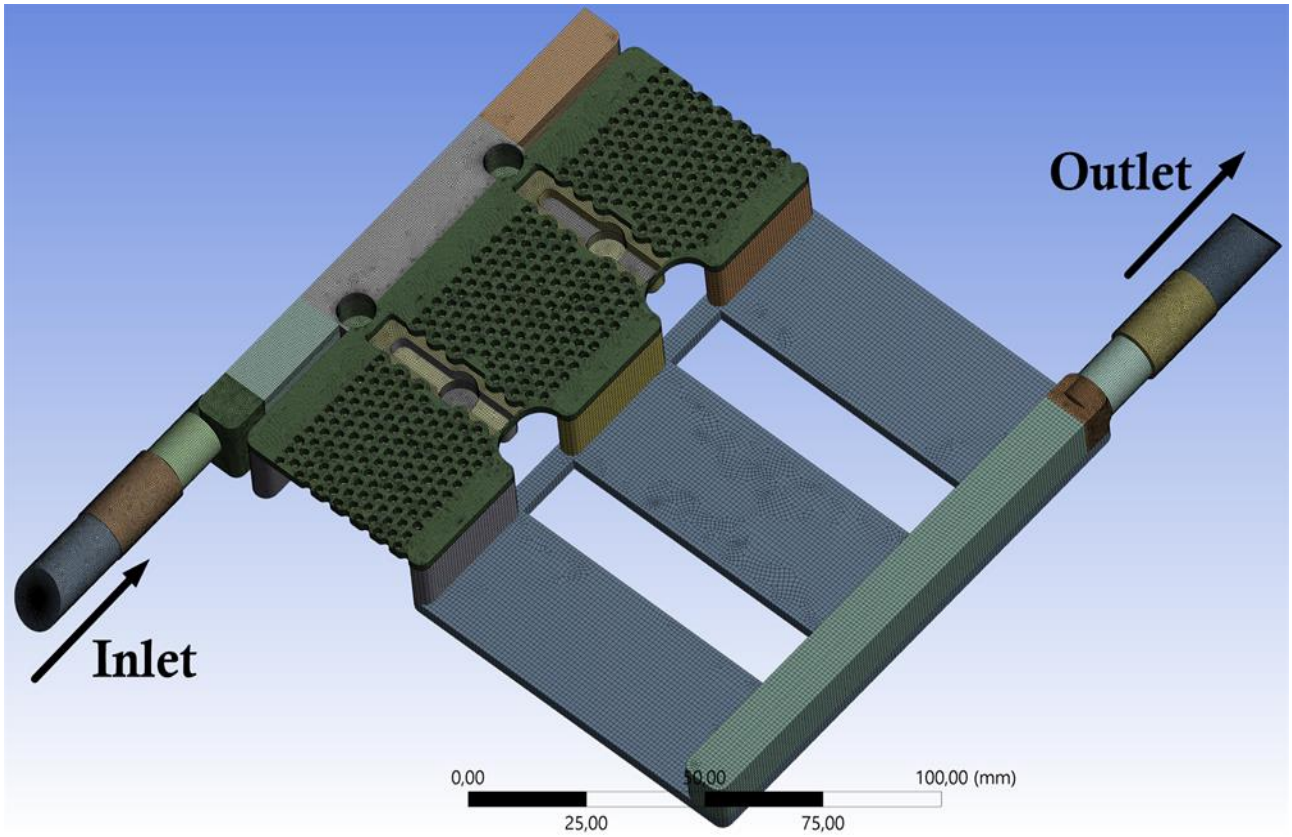

Figure 13: redesigned final fluid region

Figure 14 depicts the CAD model of the final inverter with the power hybrids on top of the copper heat sink and the fluid region beneath. The aluminium housing surrounding the fluid region is hidden.

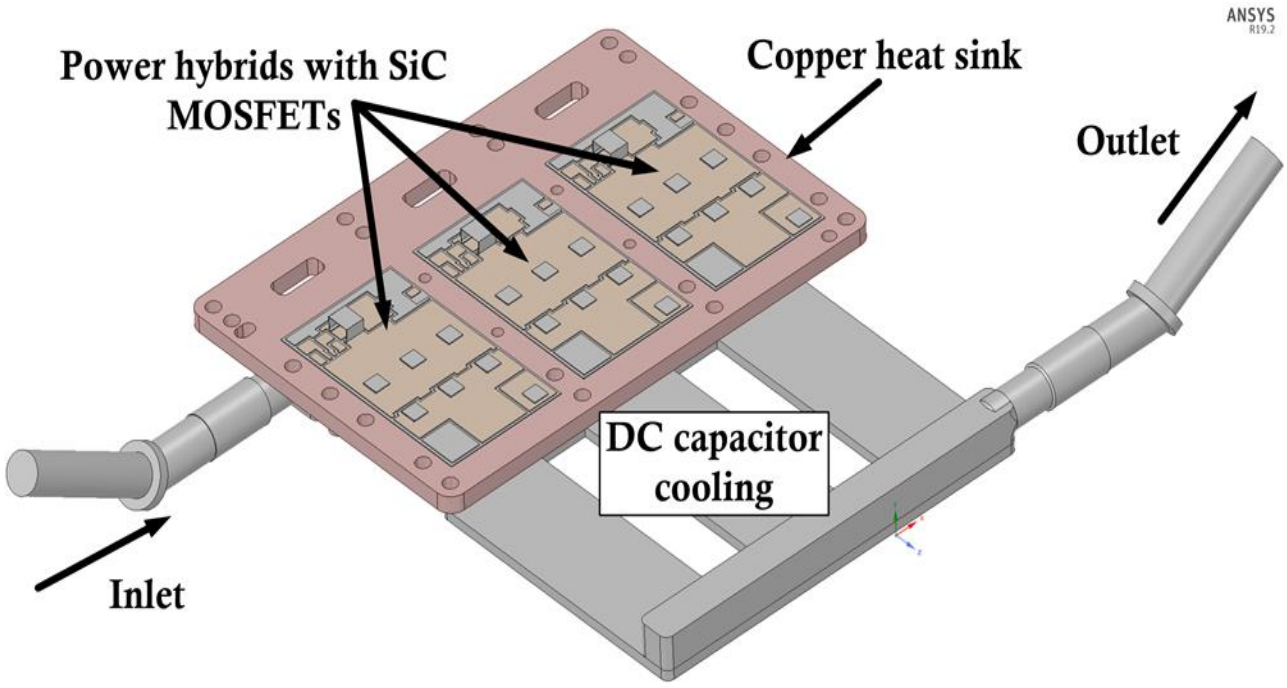

Figure 14: CAD model of the final inverter without aluminum housing

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Since the inverter design was finished a Rth investigation was done to identify the contribution of the different optimization steps.

- The thermal resistance of the first design (last report version 1): Rth = 0.92 W/K
- Optimized MOSFET distance of 8 mm: Rth reduction of 16.2%
- SiN ceramic substrate and high performance thermal paste: Rth reduction of 7.7%
- Cu heat with pin fins beneath hotspots: Rth reduction of 11.25%
- Thermal resistance of the final design: Rth = 0.625 W/K

The presented optimizations achieved a significant Rth reduction of 32.1 %. These optimizations allowed to utilize only 3 instead of 4 chips and as a result decreased the cost of the inverter by about 30%.
At this point it was interesting to compare the temperatures of the inverter with 3 chips and a 4 chip version via simulation. The version with 4 chips had a chip distance of 1 mm and the same boundary conditions as the 3 chip version (see chapter 2.1). The space consumption of the 3 and 4 chip version are compared in figure 15 with an exemplary model.

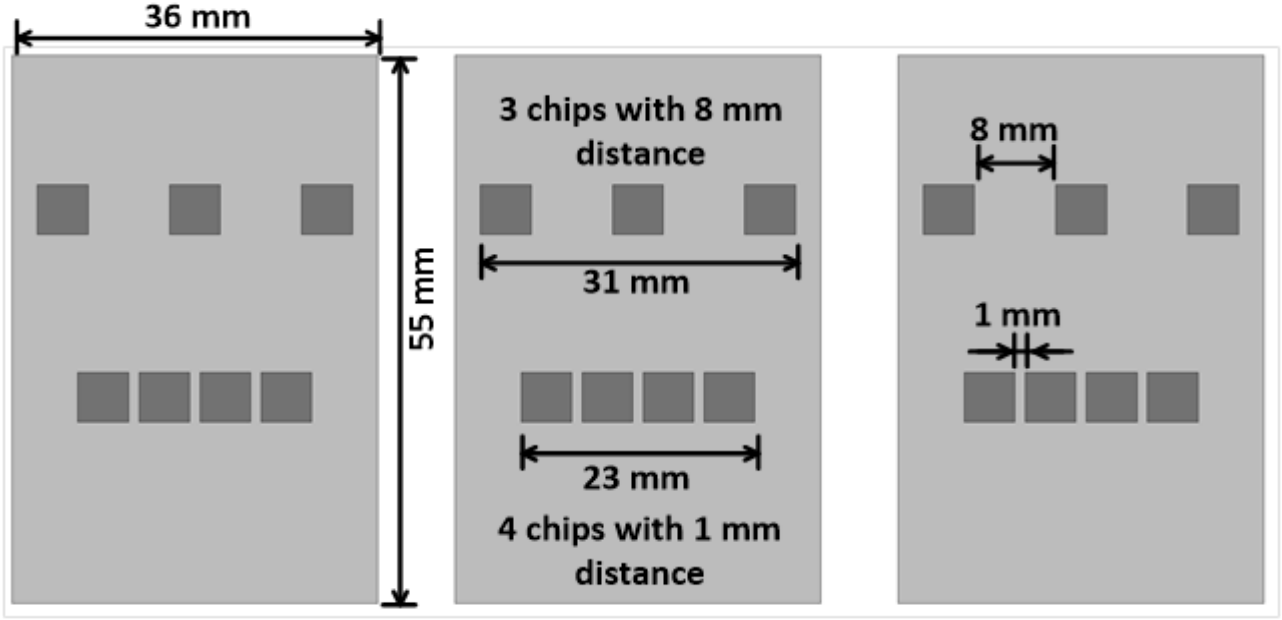

Figure 15: exemplary CAD model to compare the space consumption of 3 and 4 chips

An interesting observation is that the 3 chips with a chip distance of 8 mm doesn't take up significantly more space than 4 chips with 1 mm spacing. Figures 16 and 17 show the temperature plots of both version. The hotspot temperature of the 3 chip version is 154.47 °C (fig. 16) and the hotspot temperature of the 4 chip is 148.73 °C (fig. 17). Comparing these hotspot temperatures it turns out the 4 chip solution does not provide a significant thermal advantage despite being far more expensive. The 3 chip version is 30 % cheaper with only 3.8 % increase in the critical hotspot temperature compared to the conventional 4 chip version. Another critical factor is that the temperatures of the 3 chip version is clearly more uniform than in the temperatures of the 4 chip version (see fig. 18). The temperature difference between the chips of the 3 chip version is 5.1 °C compared to the 4 chip version with a temperature difference of 11.5 °C. Therefore, it is more beneficial to use 3 chips with a distance of 8 mm instead of 4 chips with the conventional distance.

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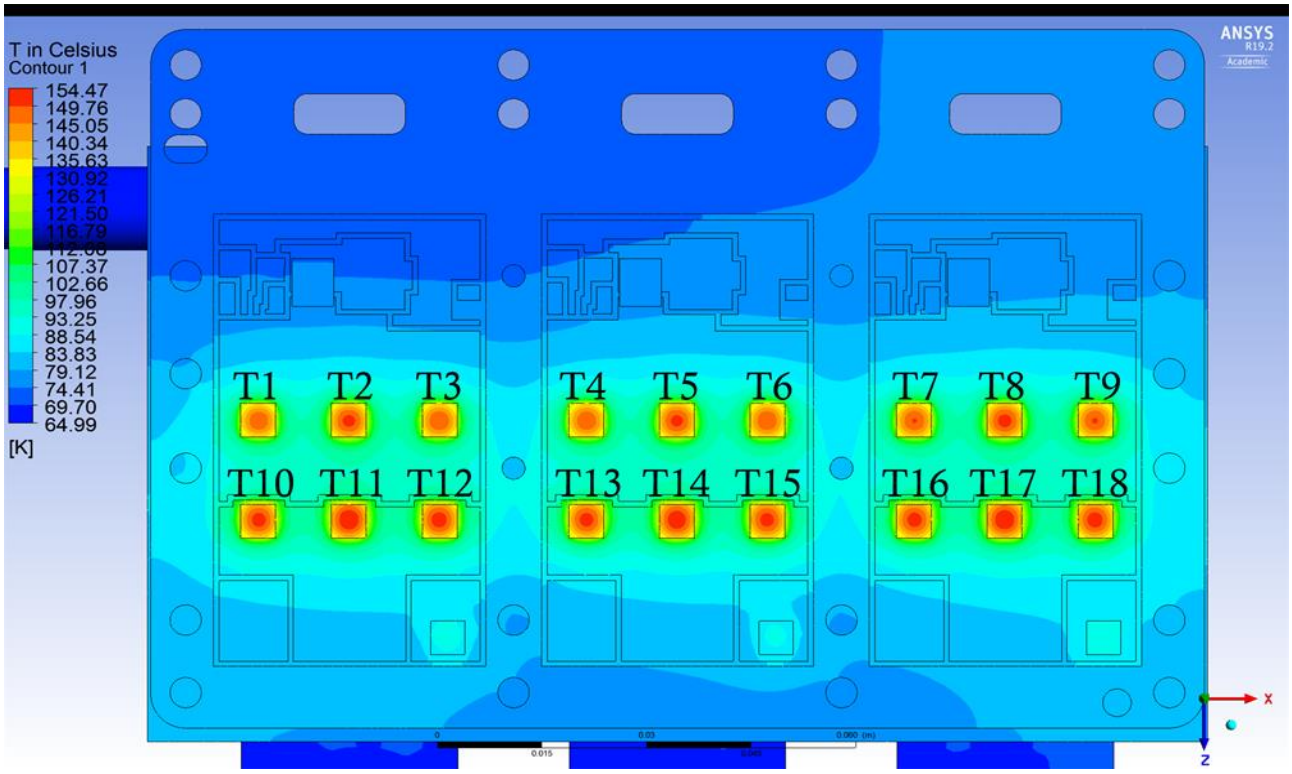

Figure 16: Thermal contour plot of the inverter with 3 chips and 8 mm distance

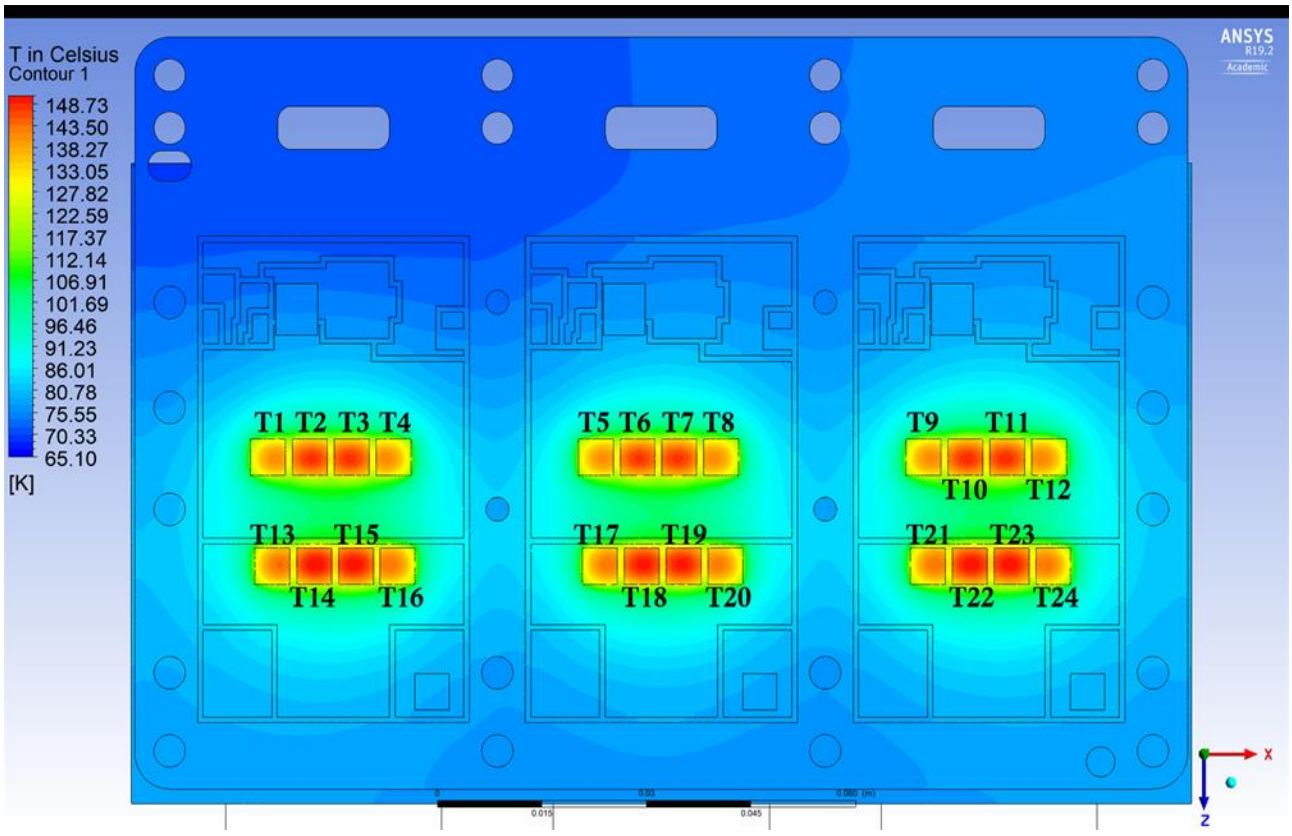

Figure 17: Thermal contour plot of the inverter with 4 chips and 1 mm distance

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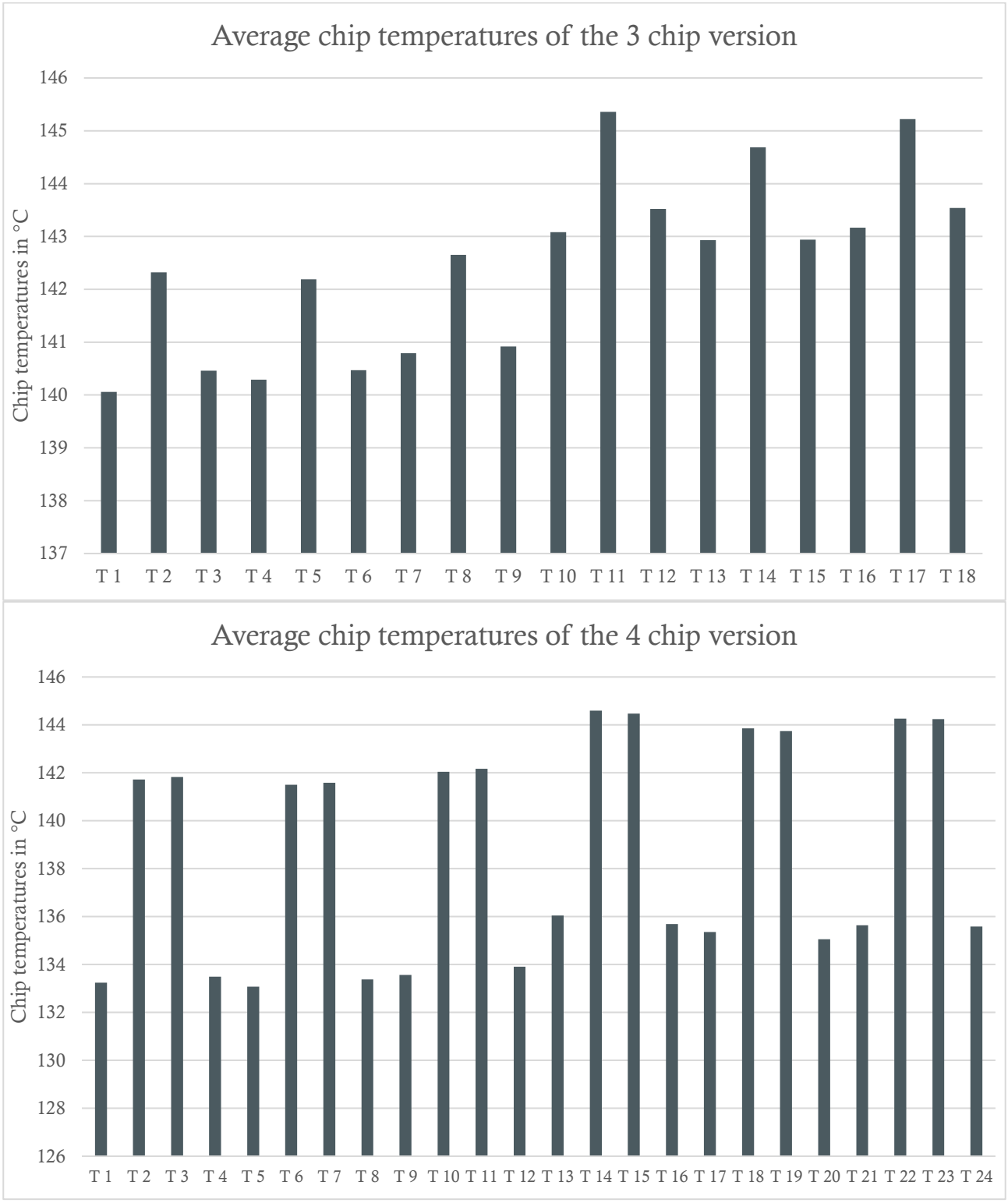

Figure 18: Graph of chip temperatures compared

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2.5 AC Layer Simulation

In addition to the presented investigations and optimizations, the influence of the flex layer on the chip temperature was investigated. This simulation was performed with ANSYS Mechanical. The flex layer could influence the chips in 3 possible ways:

1. The flex layer heats the chip. Because the flex layer too carries the 140 A there was the possibility that the losses in the current path heat up the layer
2. The flex layer could cool the chips because it offers an additional heat path on top of the chips. This is the desired possibility.
3. There is no significant influence.

Figure 19 depicts the CAD model used for the simulation. Because this simulation was intended to get a first impression of the behaviour, the model has been simplified in order to keep the complexity of the simulation and thus the computing time as low as possible.
The applied boundary conditions are depicted in figure 19. The current from the AC-link was 140 A and the DC-link current was 70 A per rail. To keep the simulation simple the chips should not be traversed by the current. Thus, the surface of all chips was set as ground. For the power loss of the chips an internal heat source with 137 W was implemented. Furthermore only 1 power hybrid was simulated and to consider the heating by the peripheral two power hybrids, dummy structures with constant temperatures were designed on top of the heat sink. Because ANSYS mechanical cannot perform fluid dynamic simulations the cooling fluid and pin structure was removed. Insead of the pin structure at the bottom of the heat sink convection with a heat transfer coefficient of 20000 W/mK was assumed.

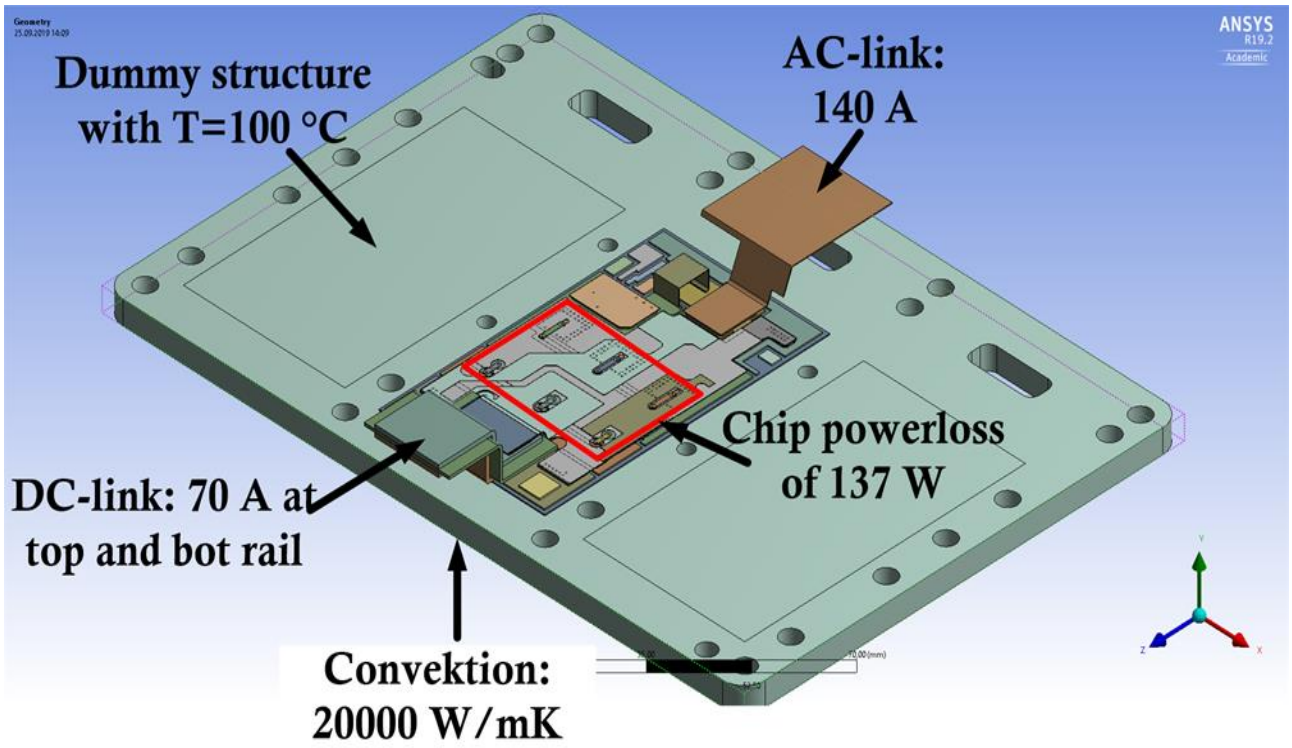

Figure 19: Simulation model of the flex layer simulation with boundary conditions

The flex layer simulation was done with three different setups. The first simulations with only the chips turned on and without a current flow through the layer. It was compared with the same

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model and setup but without a flex layer attached to it (see fig. 20 and 21). The goal was to see if there is any passive cooling effect of the flex layer on the chips.
The second simulation setup was with only the current through the flex layer. This was to investigate the self-heating of the layer and possible cooling issues. Because the layer is connected to the heat sink only via the sinter points on top of the power hybrid (see fig. 22).
The third simulation was with the heated chips and the current flow through the layer. In this simulation it could be investigated whether the layer heats or cools the chips (see fig. 23). Figures 20 to 23 depict the thermal contours of the simulation results. In all pictures the flex-layer is hidden above the chip area to show the chip temperatures.

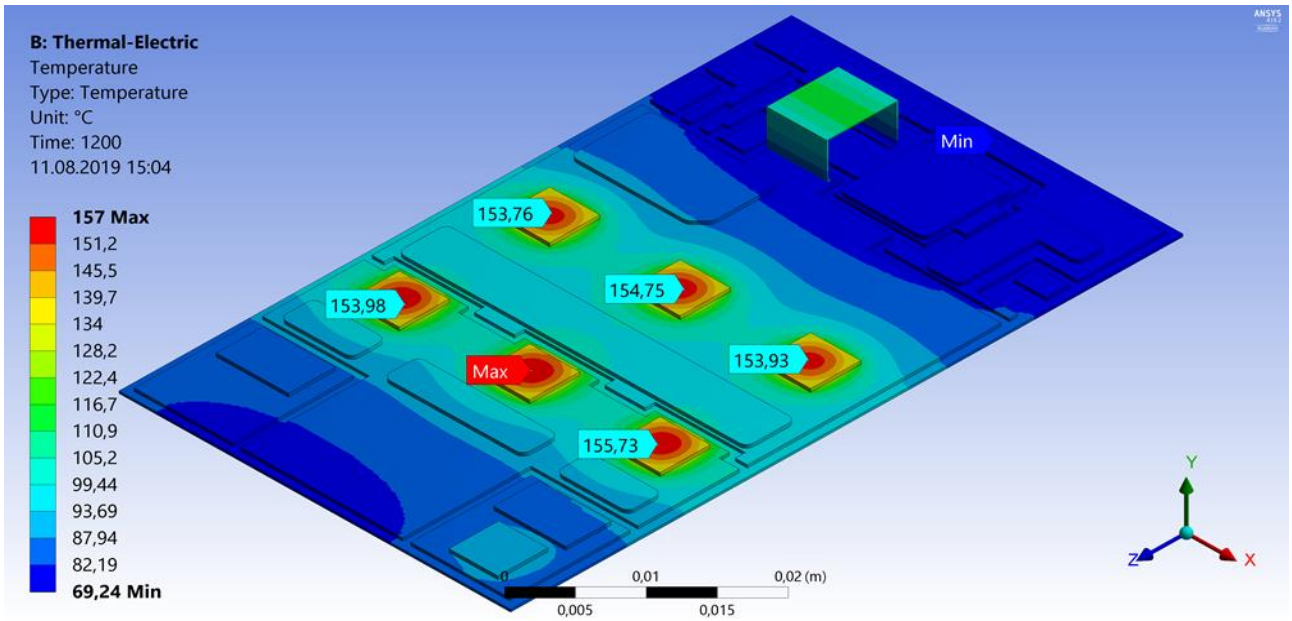

Figure 20: AC-layer simulation with only heated chips and without the flex layer

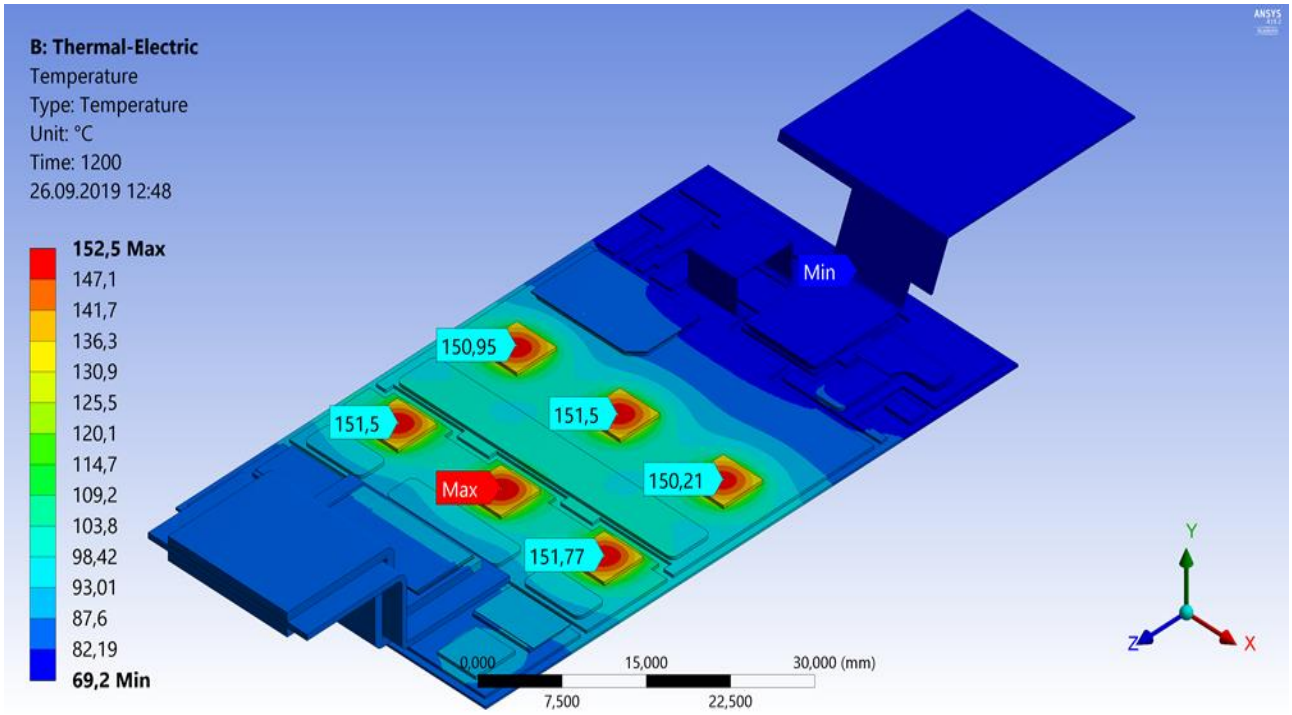

Figure 21: AC-layer simulation with only heated chips and with the flex layer

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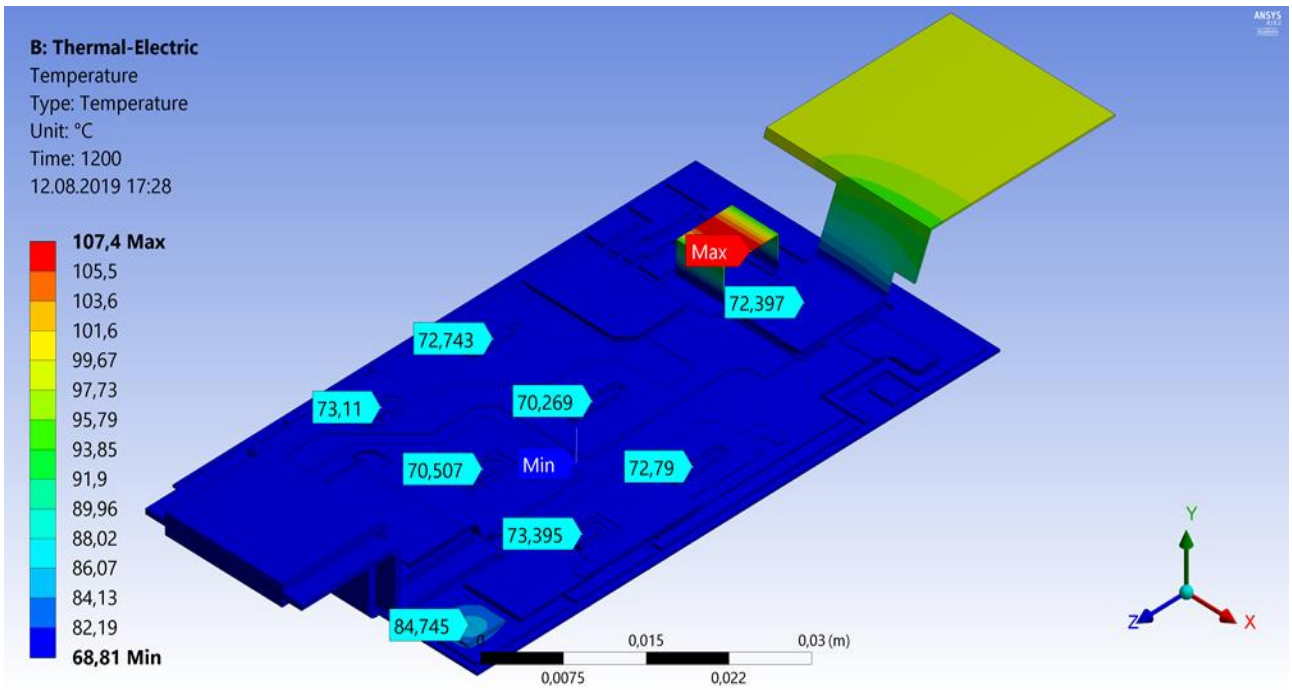

Figure 22: AC-layer simulation with only current through the flex layer

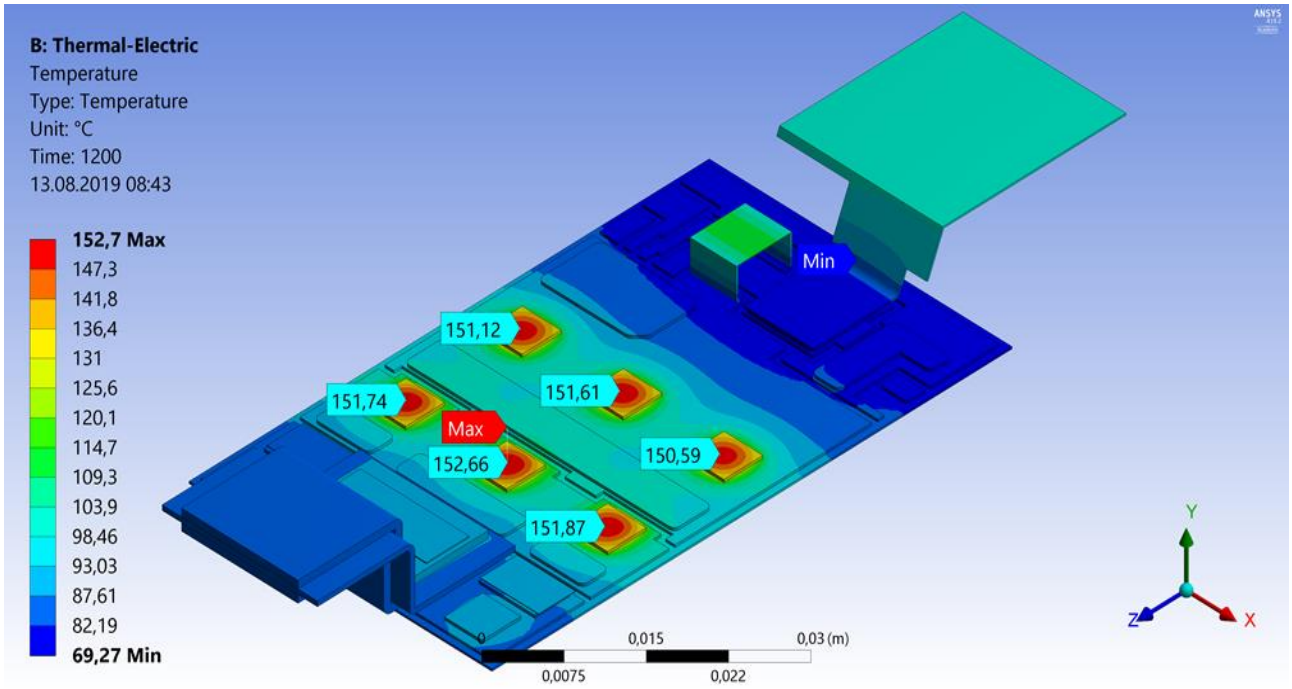

Figure 23: AC layer simulation with heated chips and current flow through the layer

Because the simulations presented in this chapter are a simplified version of the previous ones the temperatures deviate by some extend. Therefore, the absolute values of the temperatures deviate from the other simulations. Nevertheless, the results show that the flex layer has a tendency to cool the chips even with a current flow of 140 A. Furthermore, the Layer is not heated up by the current flow because of the good cooling connection via sinter points (see fig. 22). With figure 20 and figure 24 in comparison it can be seen that the layer cools the hotspot by 4.3 °C and the overall chip temperature is reduced by 4 °C. This indicates that it is rewarding to ensure a good cooling connection of the flex layer. Further the self-heating of the flex layer is

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negligible. In the future there will be a more complex simulation to further investigate this influence and the possible potential in further improving the thermal performance.

2.7 Conclusion

The thermal optimizations were continued and the thermal performance of the inverter could be further improved. An interesting interaction between the chips and the overlap with the chips was detected, but not further investigated because the matter was too complex and time consuming at this point and design stage.
The thermal characterization has shown that the thermal performance of the inverter is heavily dependent on the inlet temperature. Therefore, it can be concluded that the performance of the inverter can be further improved if higher level cooling circuit can provide a lower inlet temperature.
The comparison between the presented inverter (3 chips with 8 mm distance) and a version with 4 chips and the conventional chip distance of 1 mm generated interesting results. The hotspot temperature of the presented inverter was not significantly higher than those of the version with 4 chips. But the temperature uniformity of the presented inverter was far better than those of the 4 chips version. Furthermore, the increased space consumption because of the 8 mm chip distance compared to the conventional 1 mm chip distance is negligible.
The results of the flex-layer simulation revealed, that the chips were cooled by the flex-layer. Even if the flex-layer has to carry a current of 140 A. Probably the additional surface for heat dissipation at the top of the chips and the good connection of the flex-layer to the heat sink has a positive effect on the chip temperature. Based on the current status, further examinations can be conducted.

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3. Summary

This report continues the thermal optimization process for the inverter in WP 4. Improvements based on the results of the previous report have been accomplished. The thermal performance of the inverter has been further improved and the whole system was finalized. Investigations on the thermal behaviour dependent on the inlet temperature and the volume flow were performed and evaluated. Properties with optimization potential were redesigned in order to better meet the required boundary conditions. Additionally, a conventional inverter with 4 chips and 1 mm chip distance was simulated and compared to the presented inverter for the DRIVEMODE. The simulations show that the thermal optimization of the inverters in the context of the project delivers good results with significant cost reduction. At last a simplified flex-layer simulation was done to investigate the influence of the flex-layer on the chips. In the future a more complex 2-ways coupled simulation of this problem will be performed to better understand the thermal interaction between the chips and the flex-layer.

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4. References

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